

MS7042M1

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CPU:

Intel Northwood/Prescott
Up to 3.6GHz (FMB1.5)

System Chipset:

PM800/PT800 (North Bridge)
VIA 8237 (South Bridge)

On Board Chipset:

BIOS -- ISA EEPROM
AC'97 Codec --CMI9761
LPC Super I/O -- W83697HF
LAN -- VIA VT6103 PHY
IEEE1394 -- VIA VT6307
CLOCK -- CY28341-3

Main Memory:

DDR * 2 (Max 2GB)

Expansion Slots:

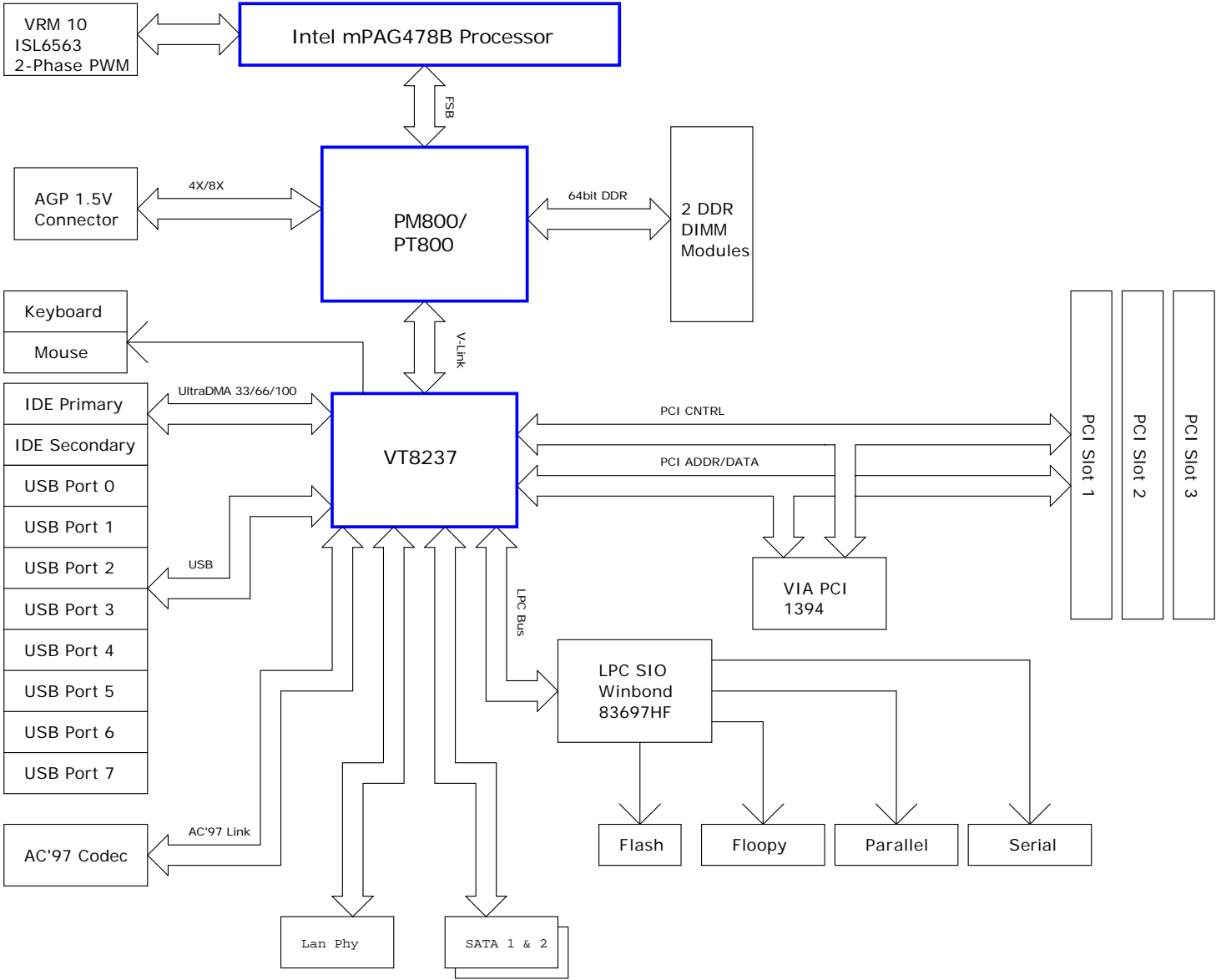
AGP * 1
PCI2.3 SLOT * 3

PWM:

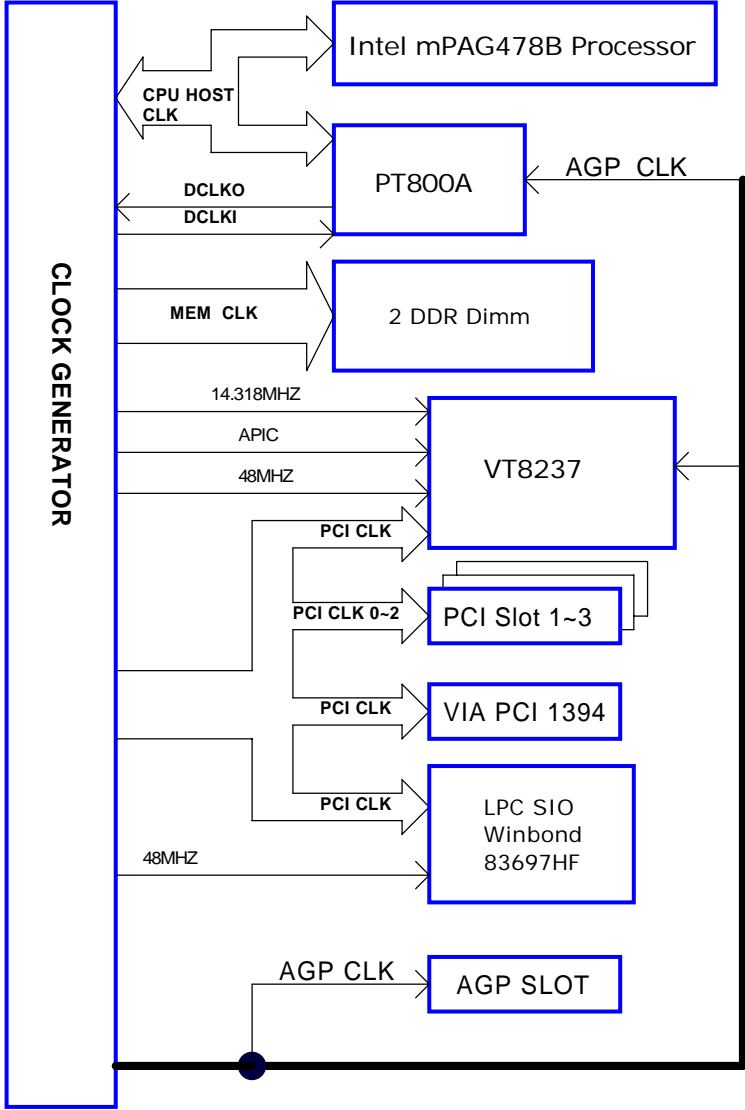
Controller: STL6710

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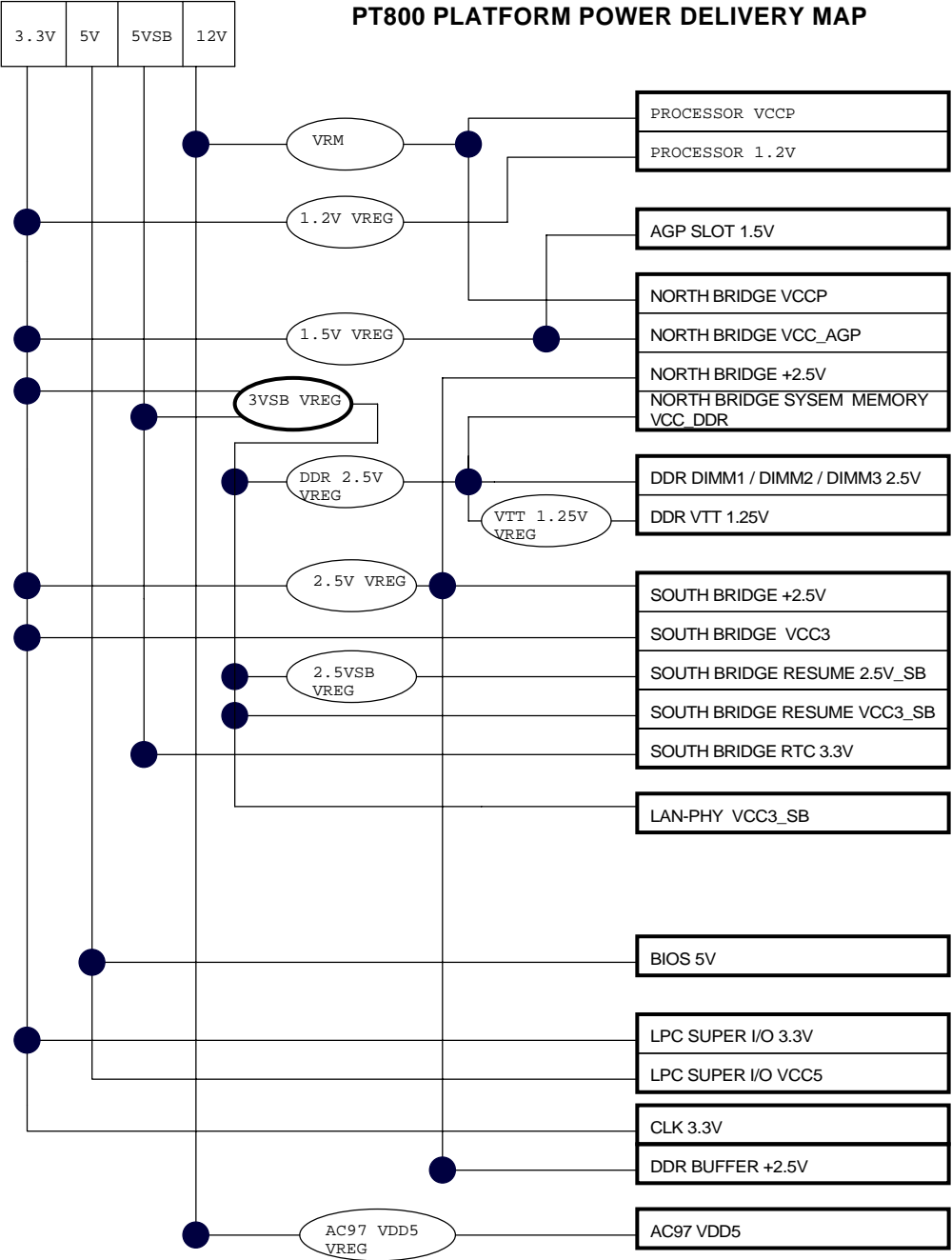
Block Diagram



PT800 PLATFORM CLOCK GENERATOR MAP



PT800 PLATFORM POWER DELIVERY MAP



SB-VT8327

GPIO Pin	Type	Function	Power well
GPI 0	I	GPI 0	RESUME
GPI 1	I	IDE2 CBD	RESUME
GPO 0	I	GPO 0	RESUME
GPO 1	I	GPO 0	RESUME
GPIO A	I	NB STR S	MAIN
GPIO B	I	IOQ DEPH	MAIN
GPIO C	I	NB STR S	MAIN
GPIO D	I	GTL PULL	MAIN

I/O-83697HF

GPIO 10	I/O	GAME GP4	MAIN
GPIO 11	I/O	GAME GP6	MAIN
GPIO 12	I/O	GAME GP2	MAIN
GPIO 13	I/O	GAME GP0	MAIN
GPIO 14	I/O	GAME GP3	MAIN
GPIO 15	I/O	GAME GP1	MAIN
GPIO 16	I/O	GAME GP7	MAIN
GPIO 17	I/O	GAME GP5	MAIN
GPIO 50	I/O	GAME TXD	MAIN
GPIO 51	I/O	GAME RXD	MAIN

DDR DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM 1	1010000B	MDCLKA0/A#0 MDCLKA1/A#1 MDCLKA2/A#2
DIMM 2	1010001B	MDCLKB0/B#0 MDCLKB1/B#1 MDCLKB2/B#2

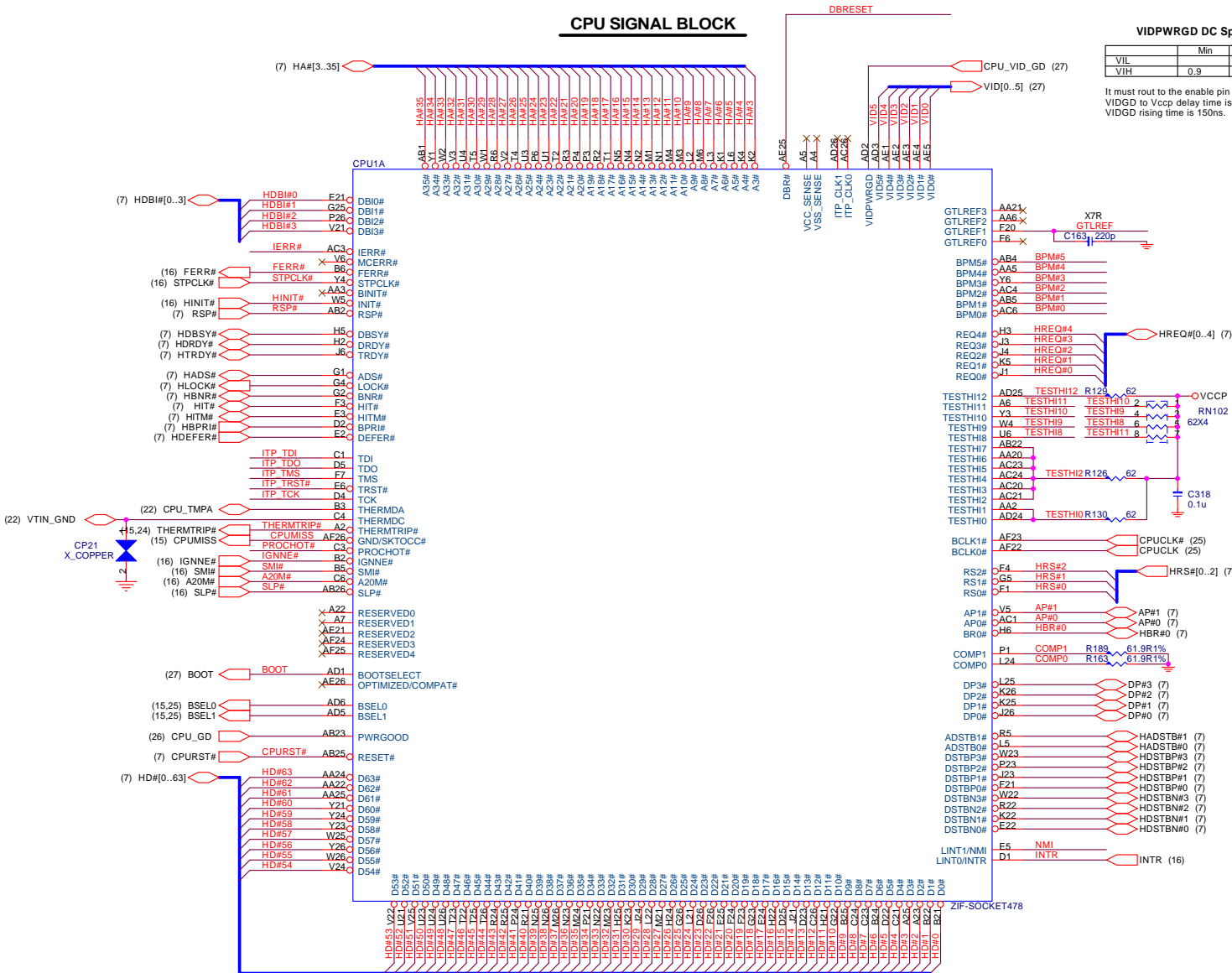
PCI Config.

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	CLK GEN PIN OUT
PCI Slot 1	PIRQ#A PIRQ#B PIRQ#C PIRQ#D	PREQ#0 PGNT#0	AD16	PCICLK0	15 (PCI_CLK0)
PCI Slot 2	PIRQ#B PIRQ#C PIRQ#D PIRQ#A	PREQ#1 PGNT#1	AD17	PCICLK1	17 (PCI_CLK1)
	PIRQ#D PIRQ#A PIRQ#B PIRQ#C	PREQ#3 PGNT#3	AD19	PCICLK3	14 (PCI_CLK1)
PCI Slot 3	PIRQ#C PIRQ#D PIRQ#A PIRQ#B	PREQ#2 PGNT#2	AD18	PCICLK2	18 (PCI_CLK2)
PCI 1394	PIRQ#E	PREQ#4 PGNT#4	AD20	1394PCLK	10(1394PCLK)

PCI RESET DEVICE

Signals	Source	Target
PCIRST#	SB	MS7, AGP slot
PCIRST#1	MS7	NB, SIO
PCIRST#2	MS7	PCI slot 1-3
DEV_RST#	MS7	PCI 1394
HDRST#	MS7	Primary, Scondary IDE

CPU SIGNAL BLOCK

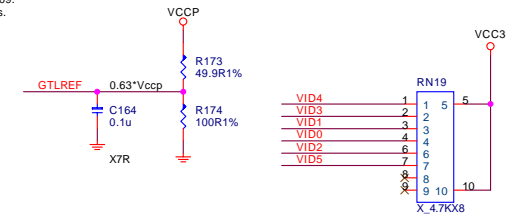


VIDPWRGD DC Specifications

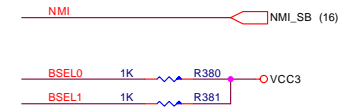
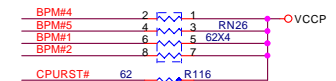
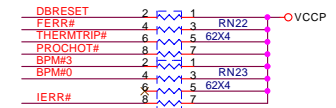
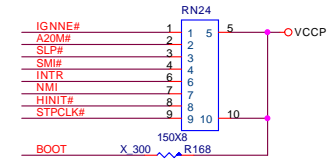
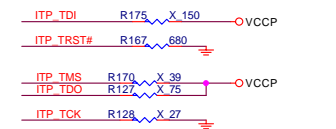
	Min	Typ	Max
VIL			0.3
VIH	0.9		

It must route to the enable pin of PWM and CK-409.
VIDGD to Vccp delay time is from 1ms to 10ms.
VIDGD rising time is 150ns.

CPU GTL REFERENCE VOLTAGE BLOCK

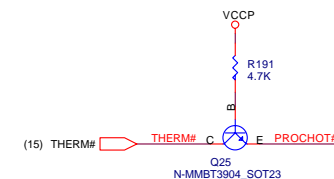
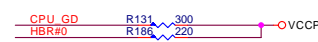


CPU ITP BLOCK

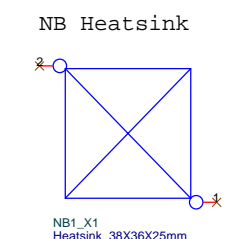
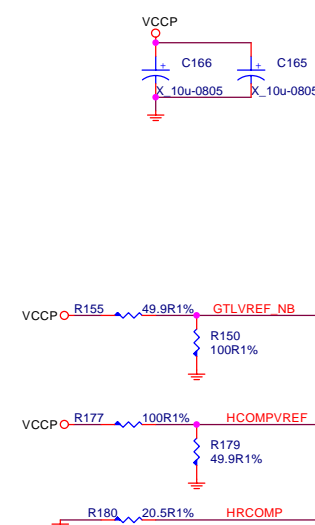
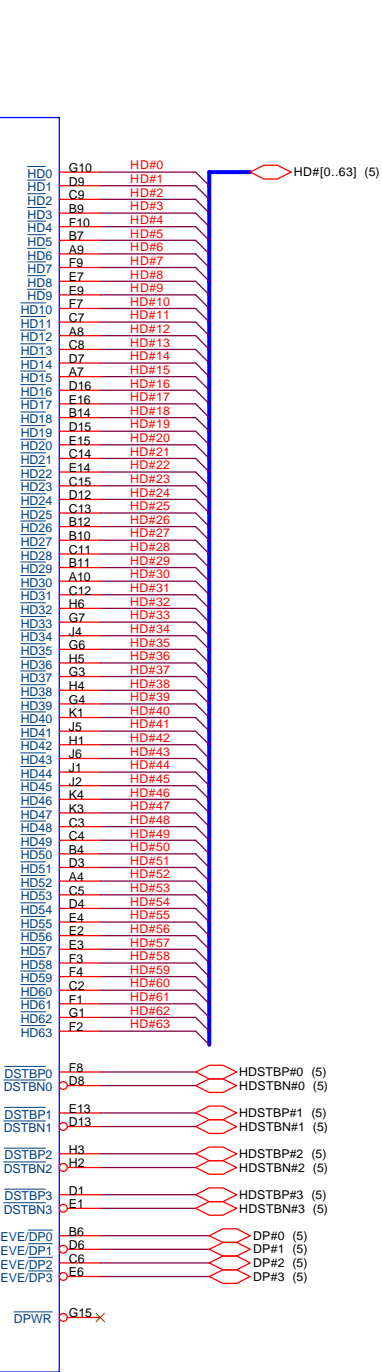
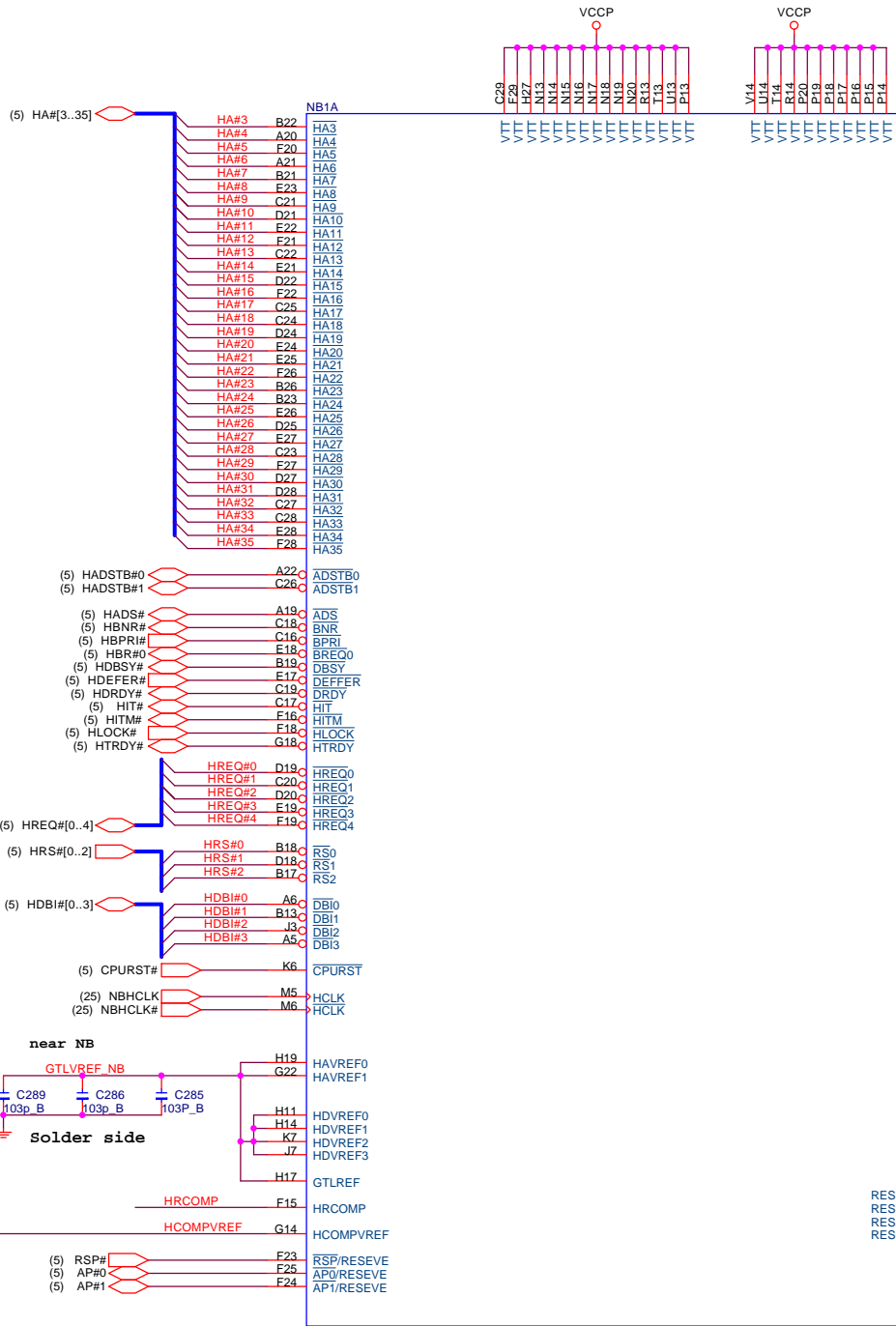


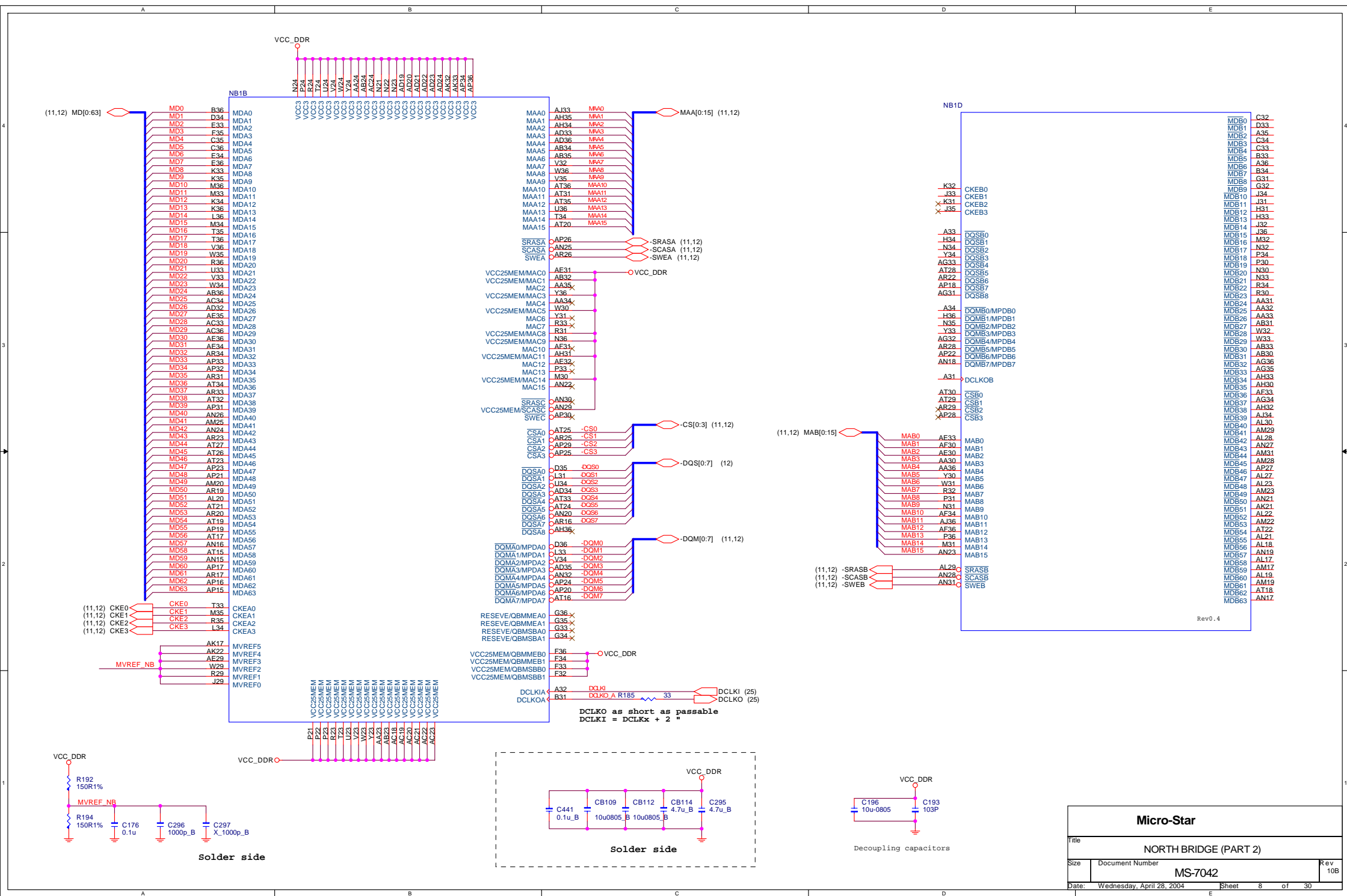
CPU STRAPPING RESISTORS

ALL COMPONENTS CLOSE TO CPU

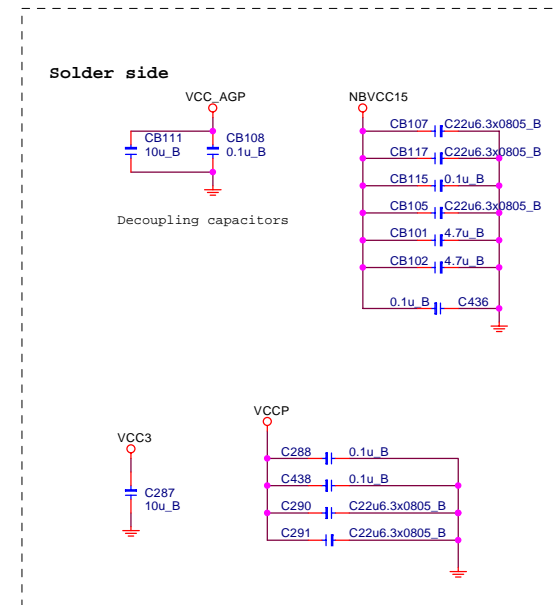
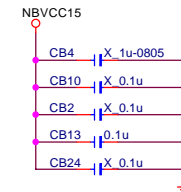


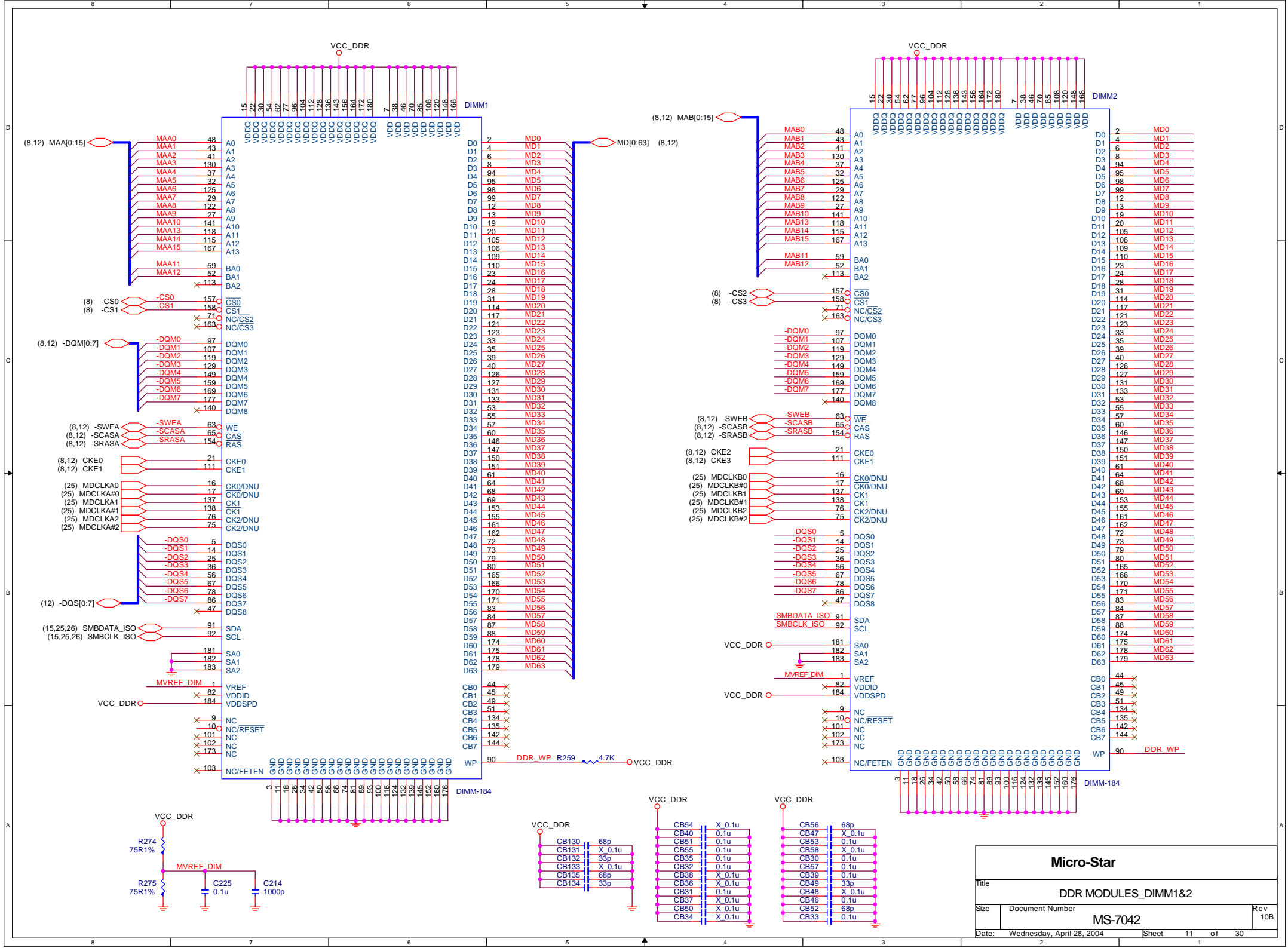
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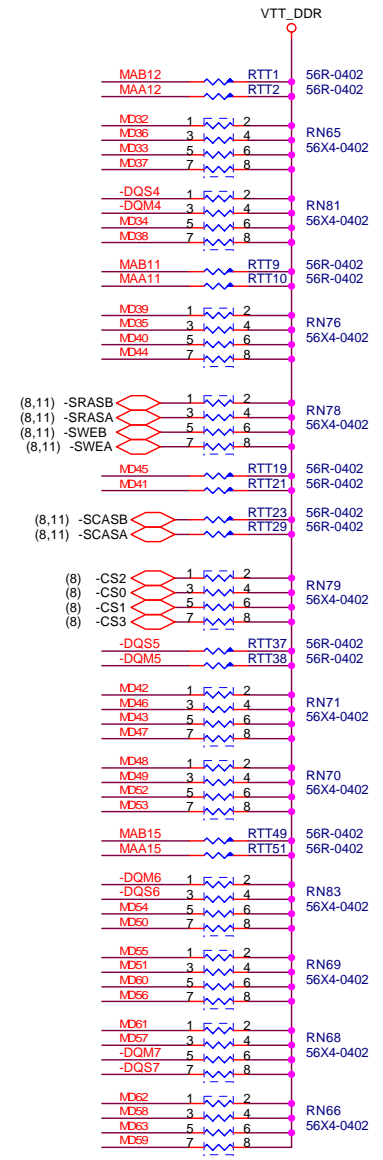
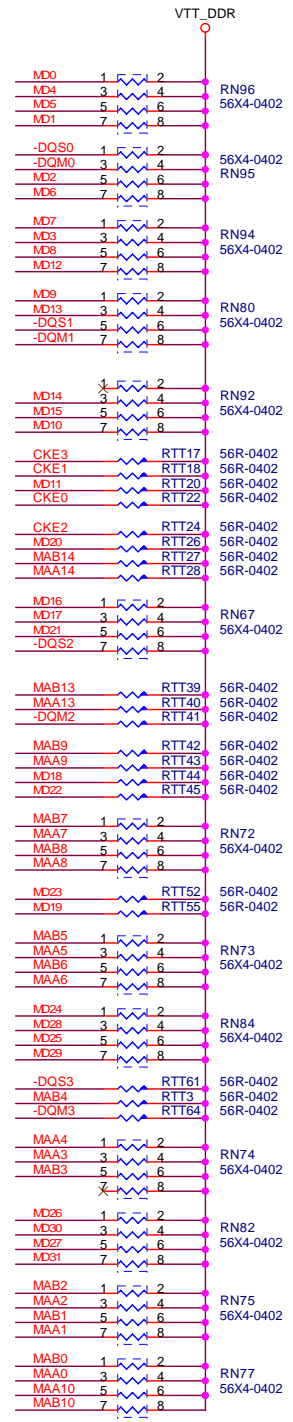
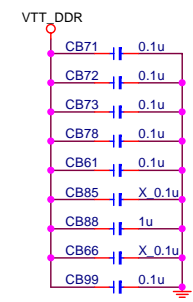
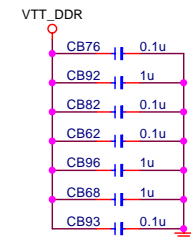
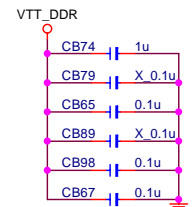
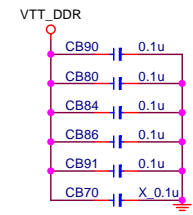
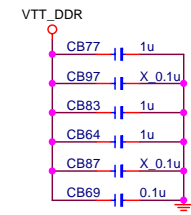
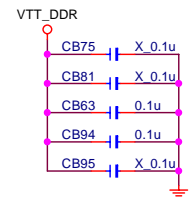
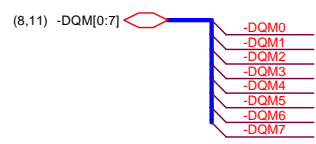
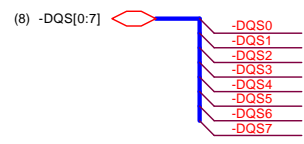
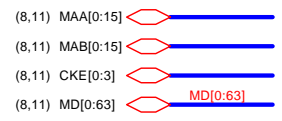




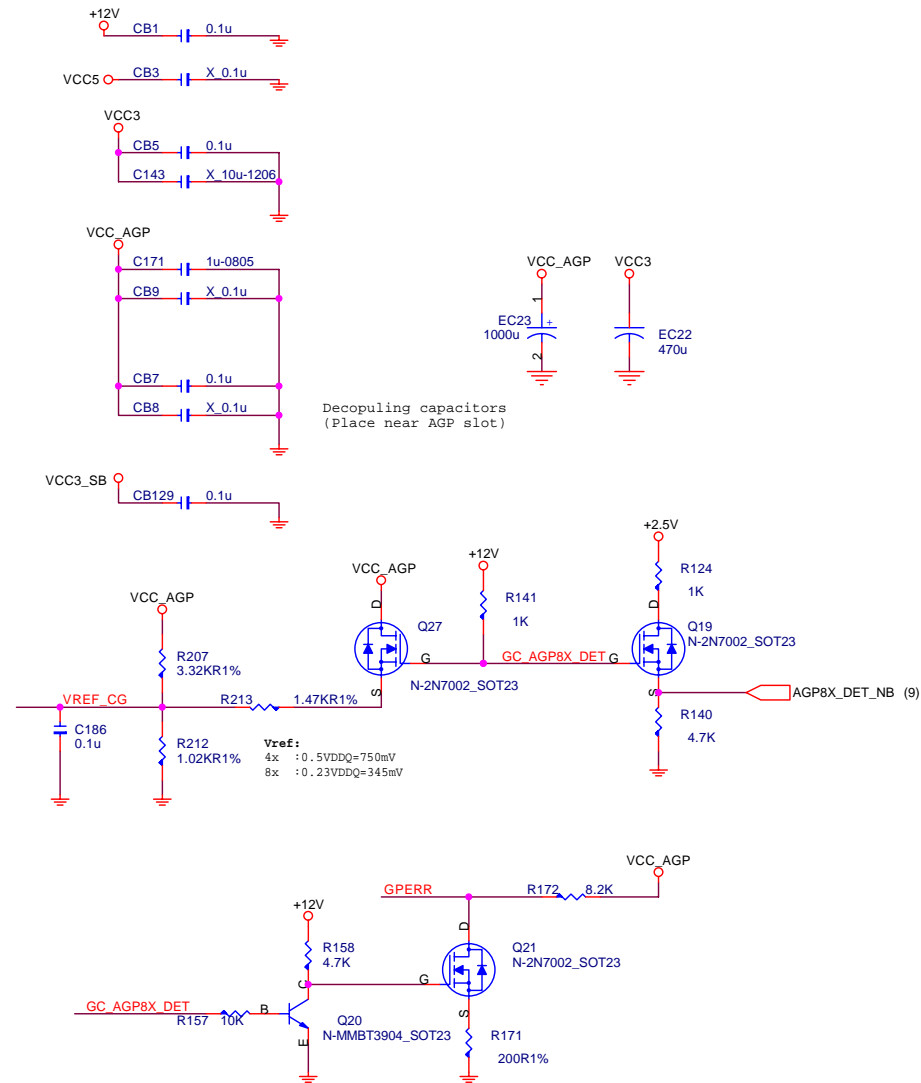
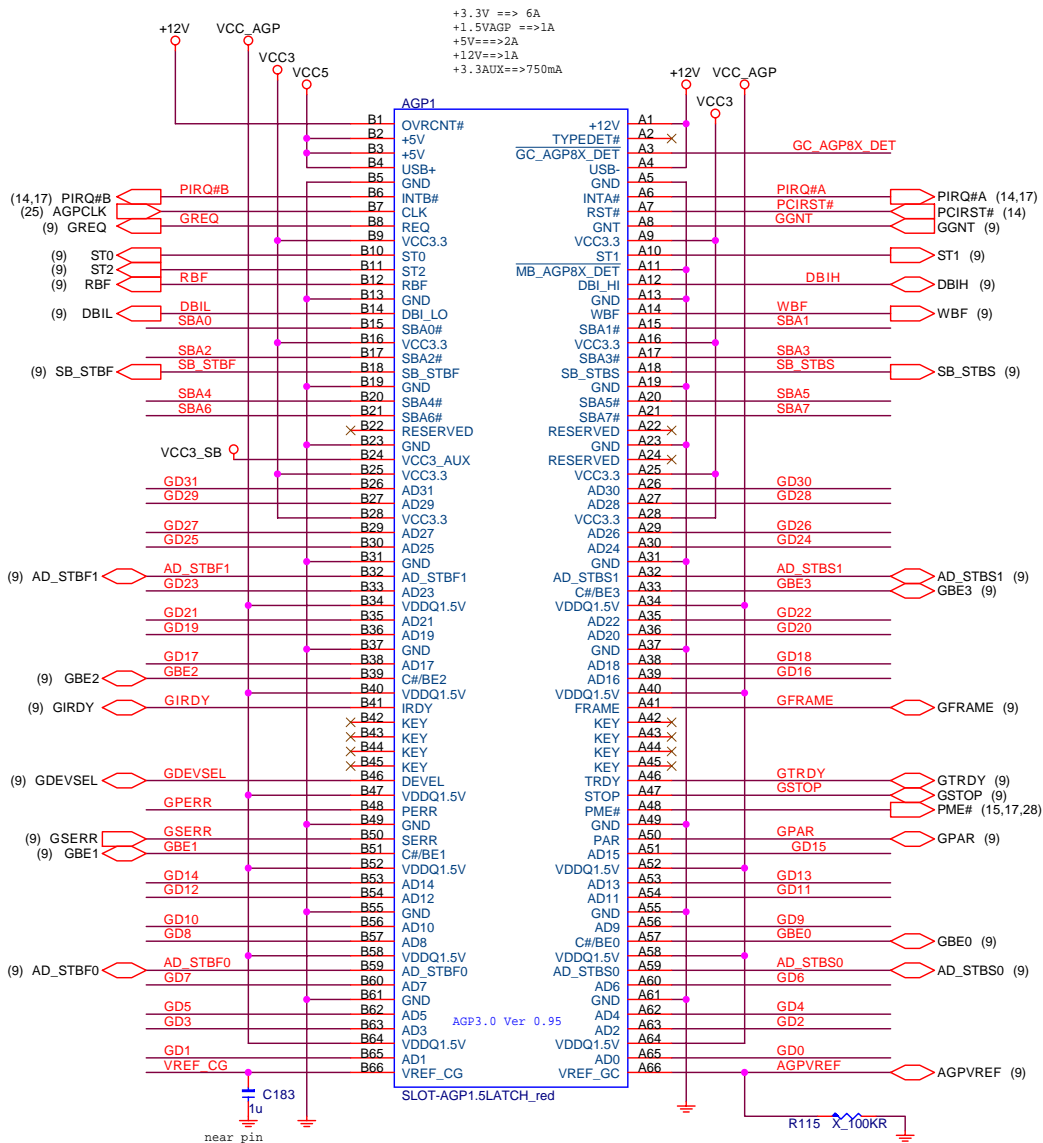






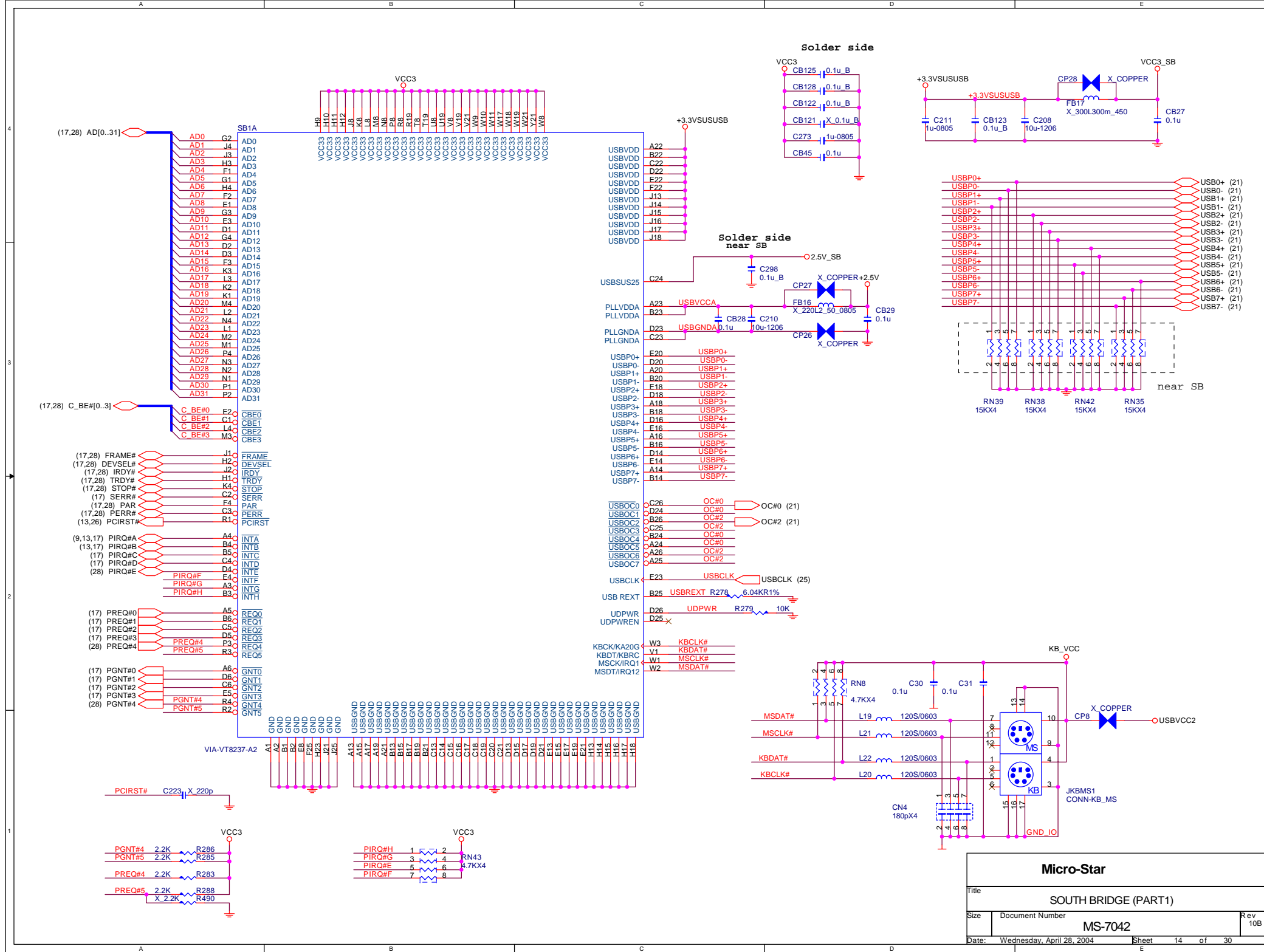


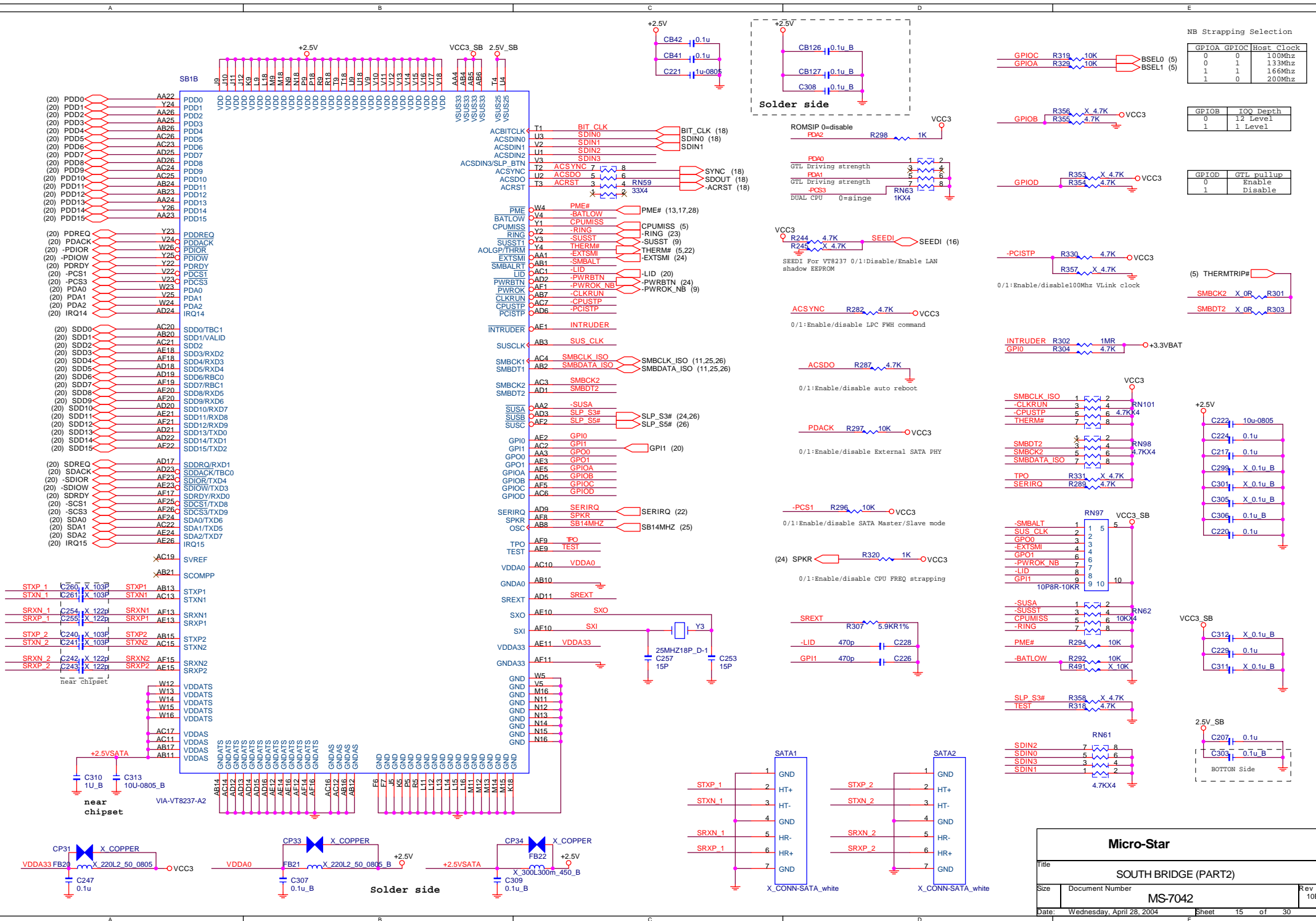
(9) SBA[0:7] SBA[0:7]
(9) GD[0:31] GD[0:31]



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NB Strapping Selection

GPIOA	GPIOC	Host Clock
0	0	100Mhz
0	1	133Mhz
1	1	166Mhz
1	0	200Mhz

GPIOB	IOQ Depth
0	12 Level
1	1 Level

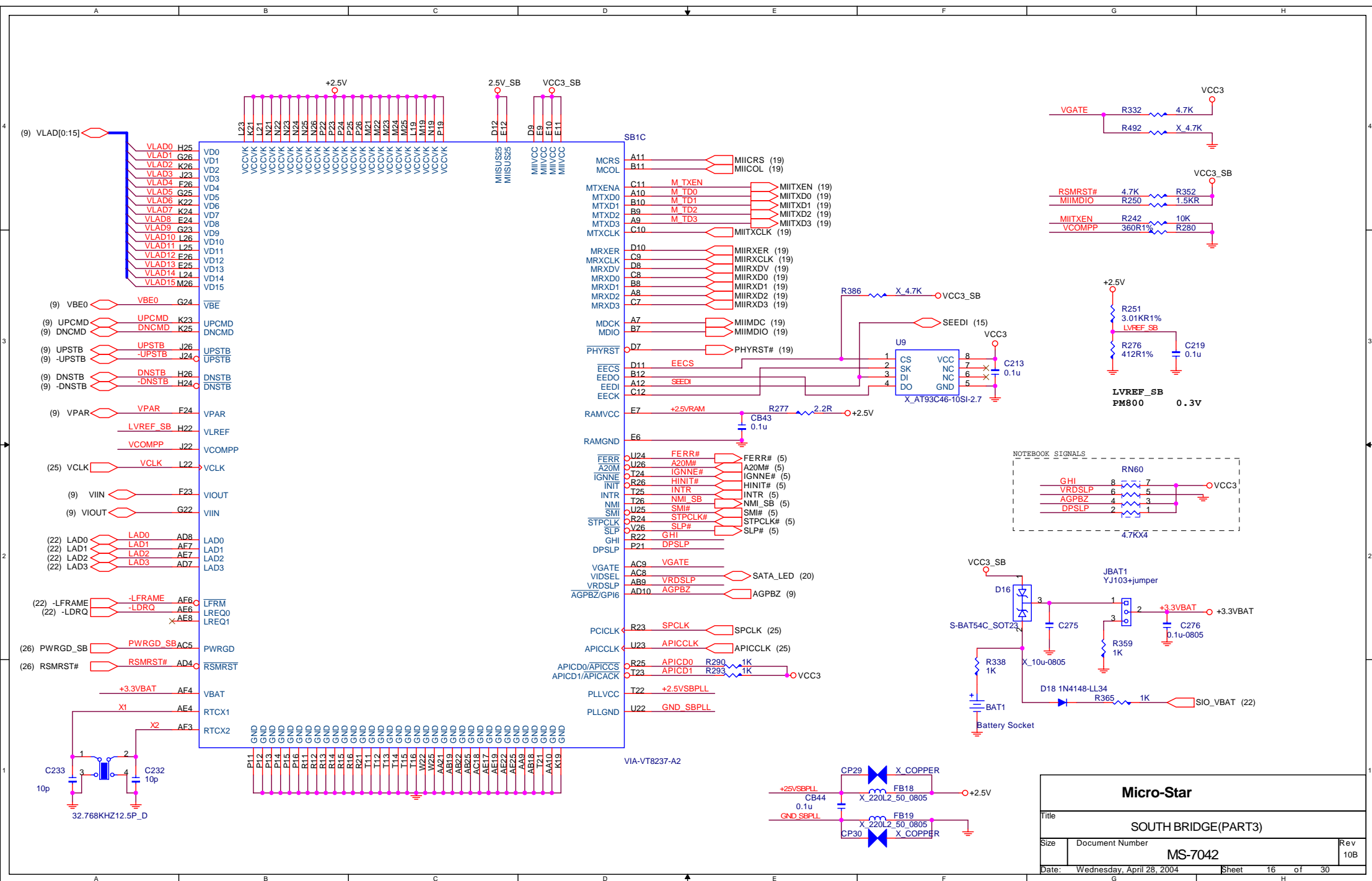
GPIOD	GTL pullup
0	Enable
1	Disable

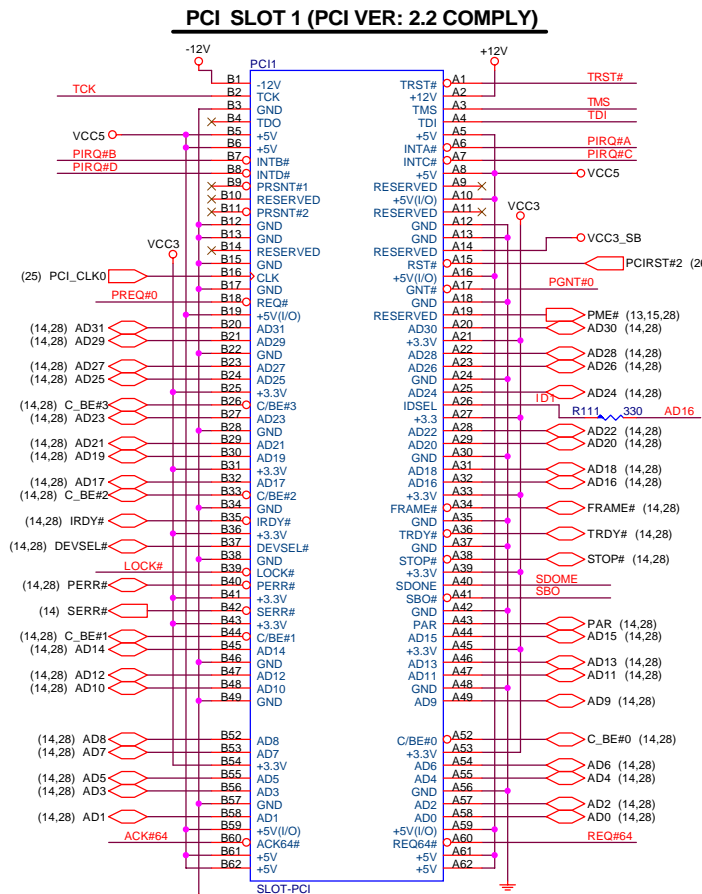
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Title: SOUTH BRIDGE (PART2)

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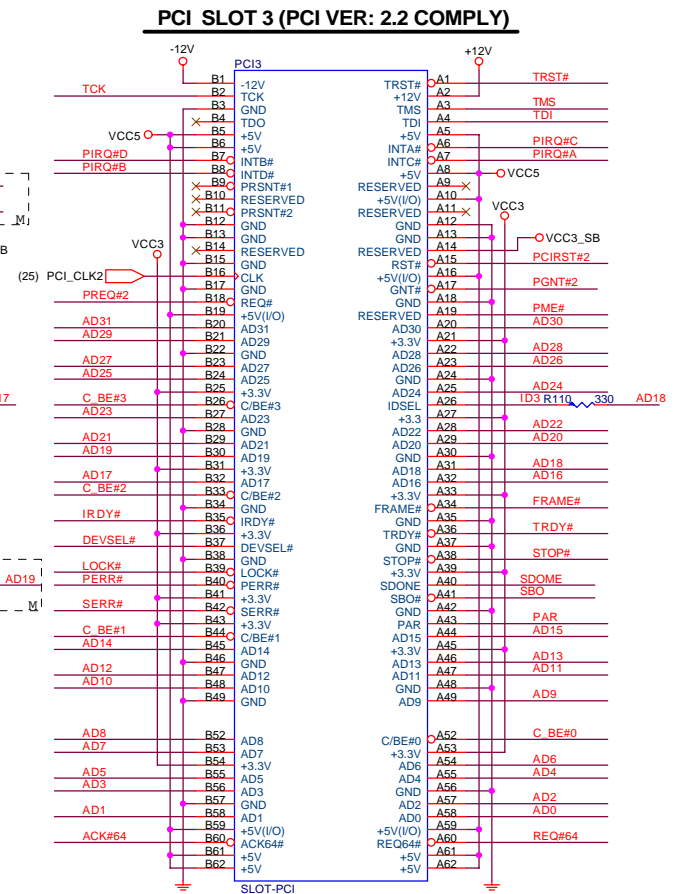




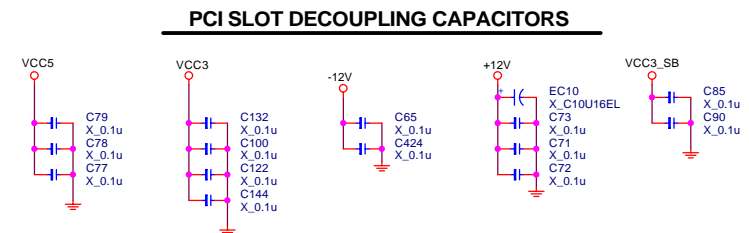
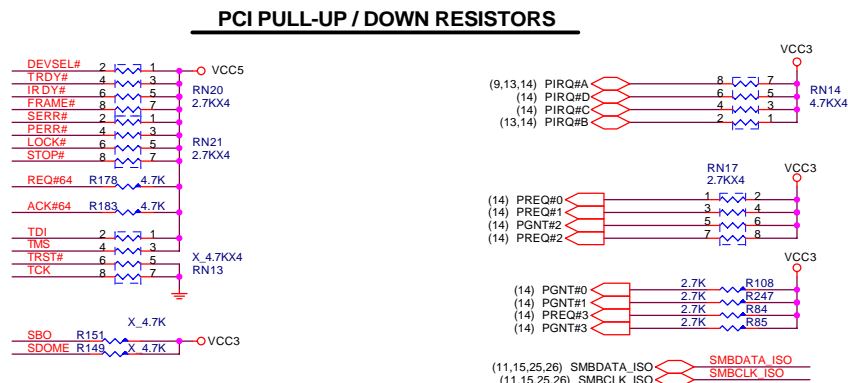
AD16, PREQ#0, PIRQ#A



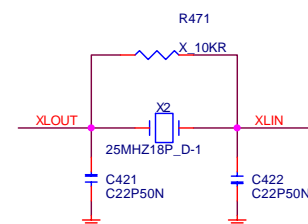
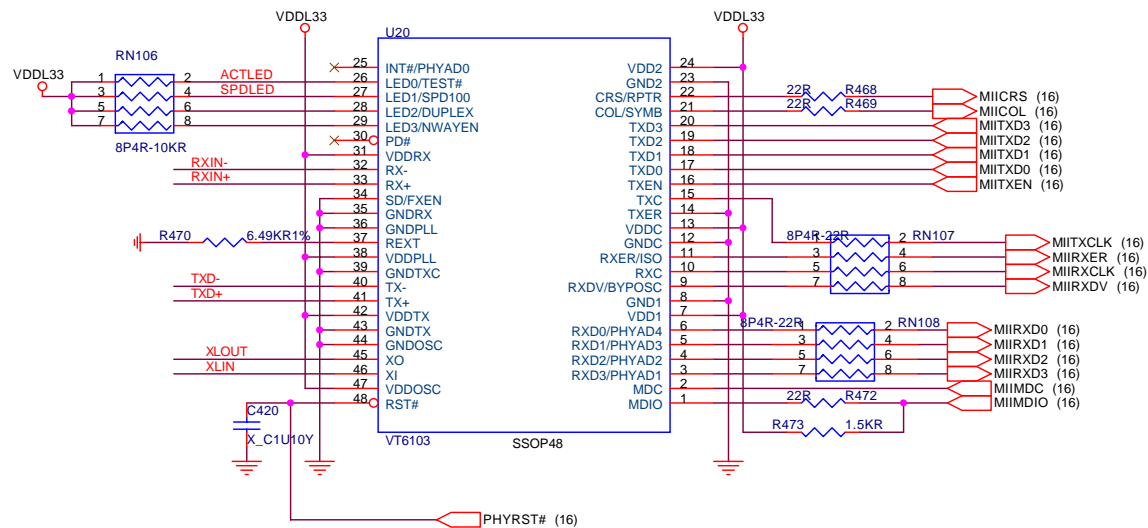
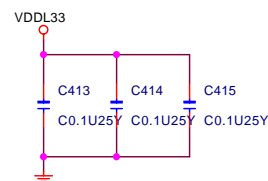
AD17, PREQ#1, PIRQ#B
AD19, PREQ#3, PIRQ#D



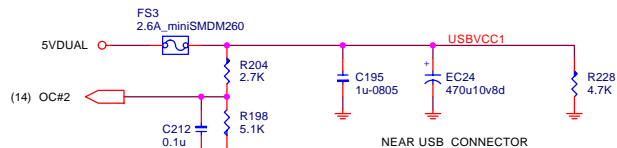
AD18, PREQ#2, PIRQ#C



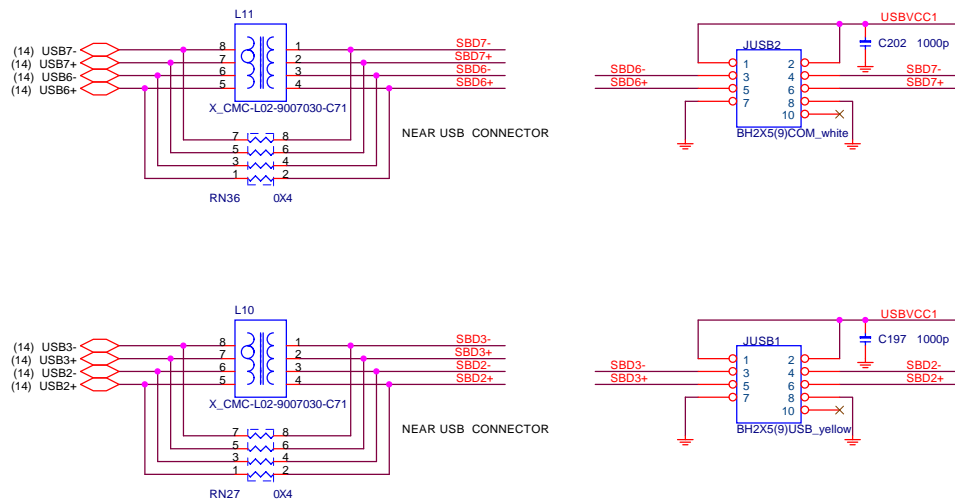
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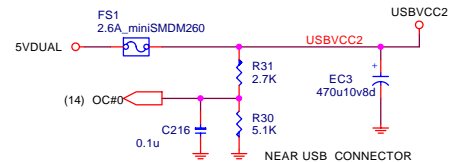
POWER CIRCUIT FOR USB PORT 4,5,6,7



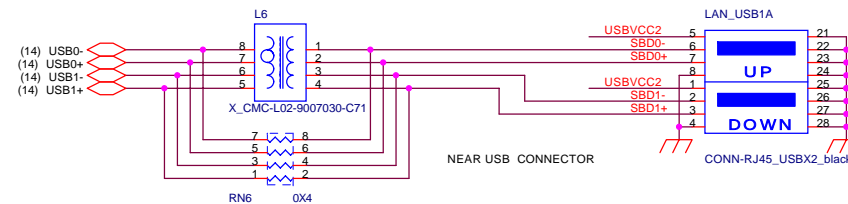
REAR PANEL USB CONNECTOR FOR USB PORT 4,5,6,7



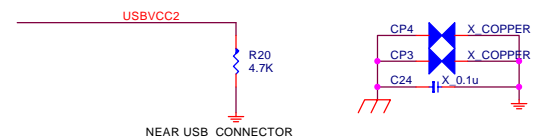
POWER CIRCUIT FOR USB PORT 2,3



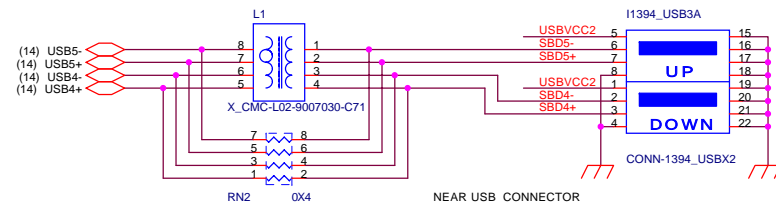
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



POWER CIRCUIT FOR USB PORT 0,1



REAR PANEL USB CONNECTOR FOR USB PORT 0,1

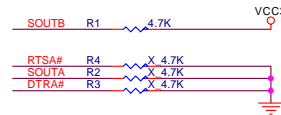


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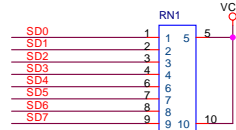
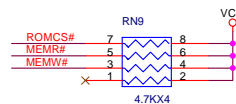
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USB Connectors		
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STRAPS

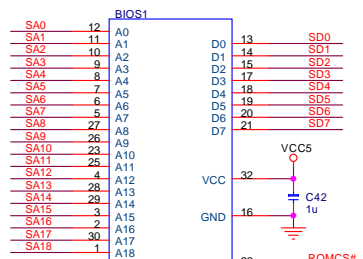
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SOUTB	L: 24MHZ	H: 48MHZ



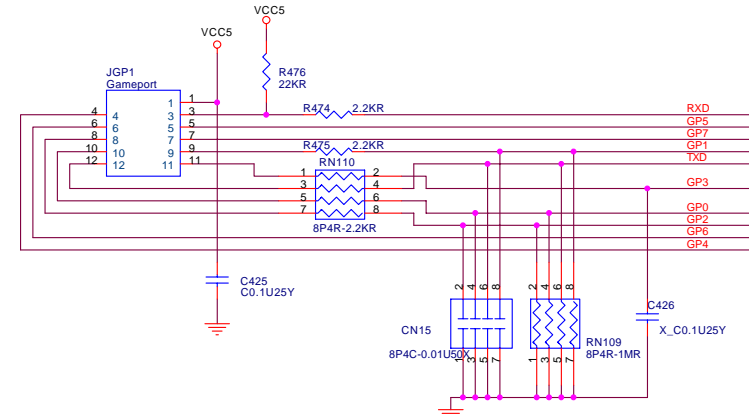
Flash Rom



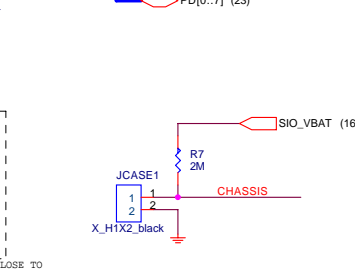
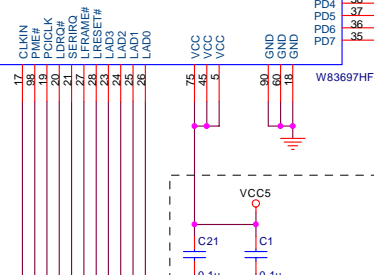
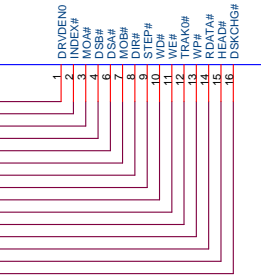
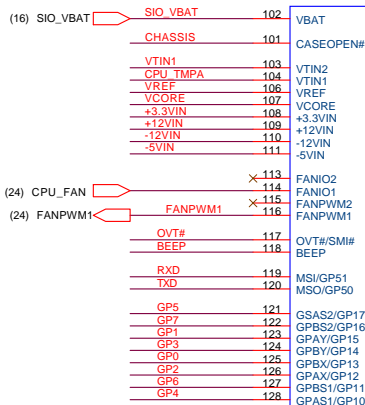
MX29F040QC-90



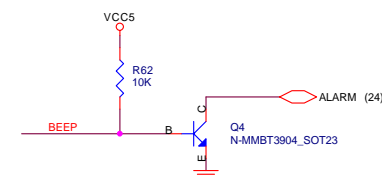
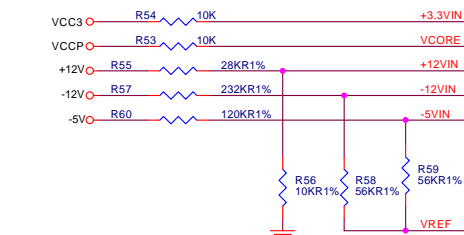
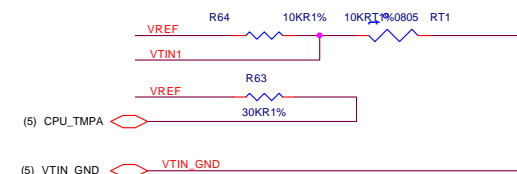
GAME PORT



W83697HF



Hardware Monitor



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Parallel Port

Serial Port

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Title Parallel/Serial Port

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Rev 10B

Parallel Port

Serial Port

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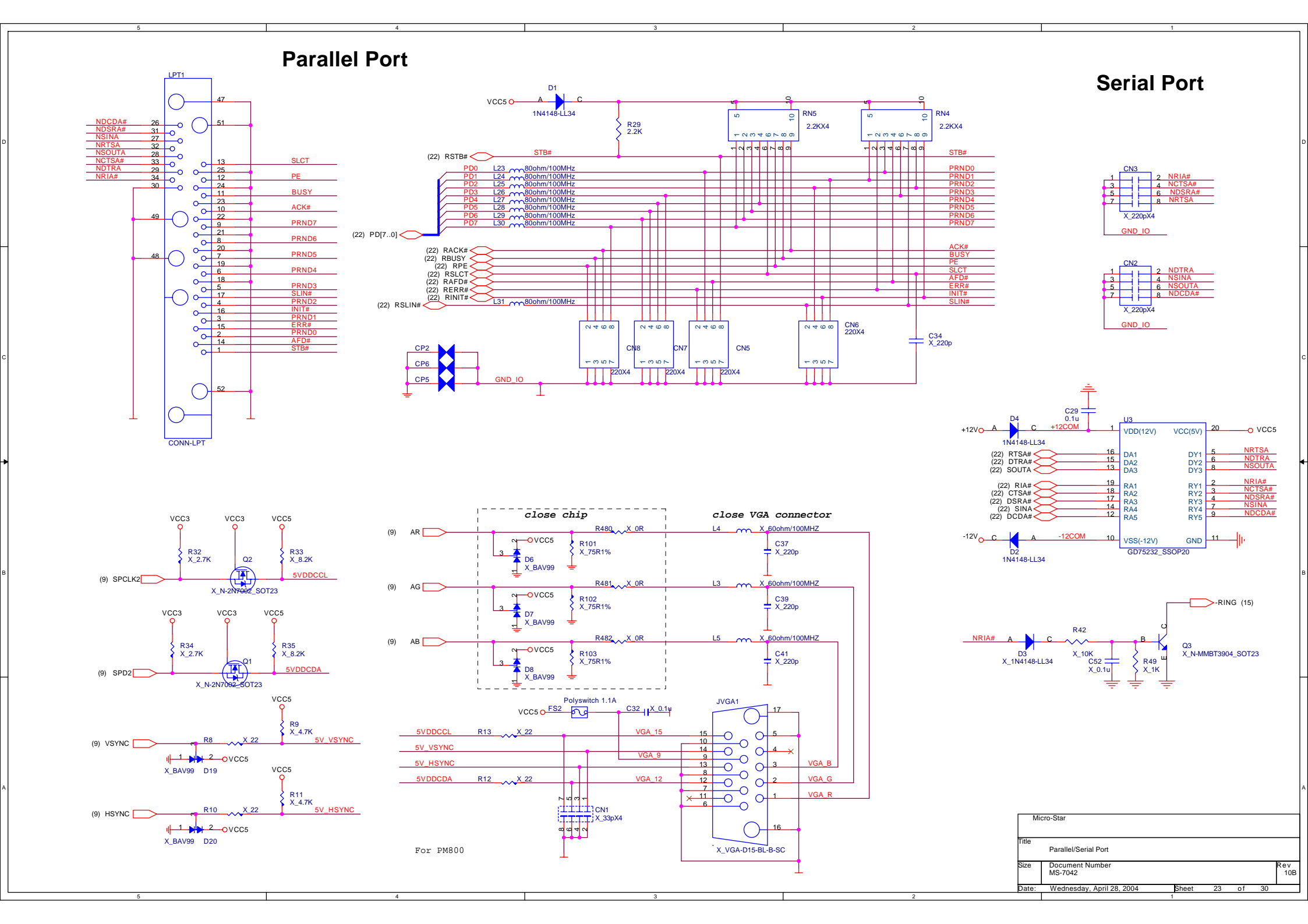
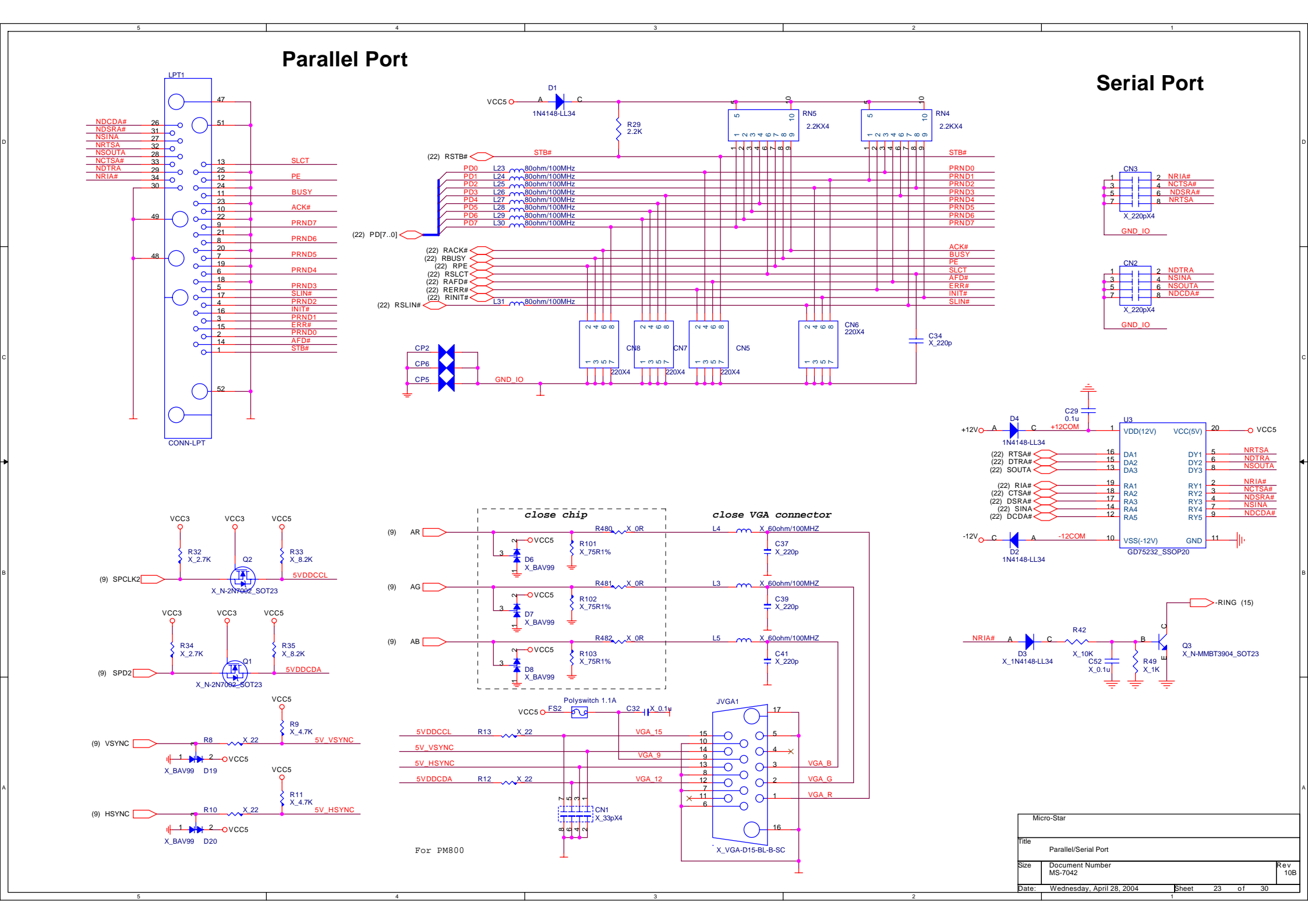
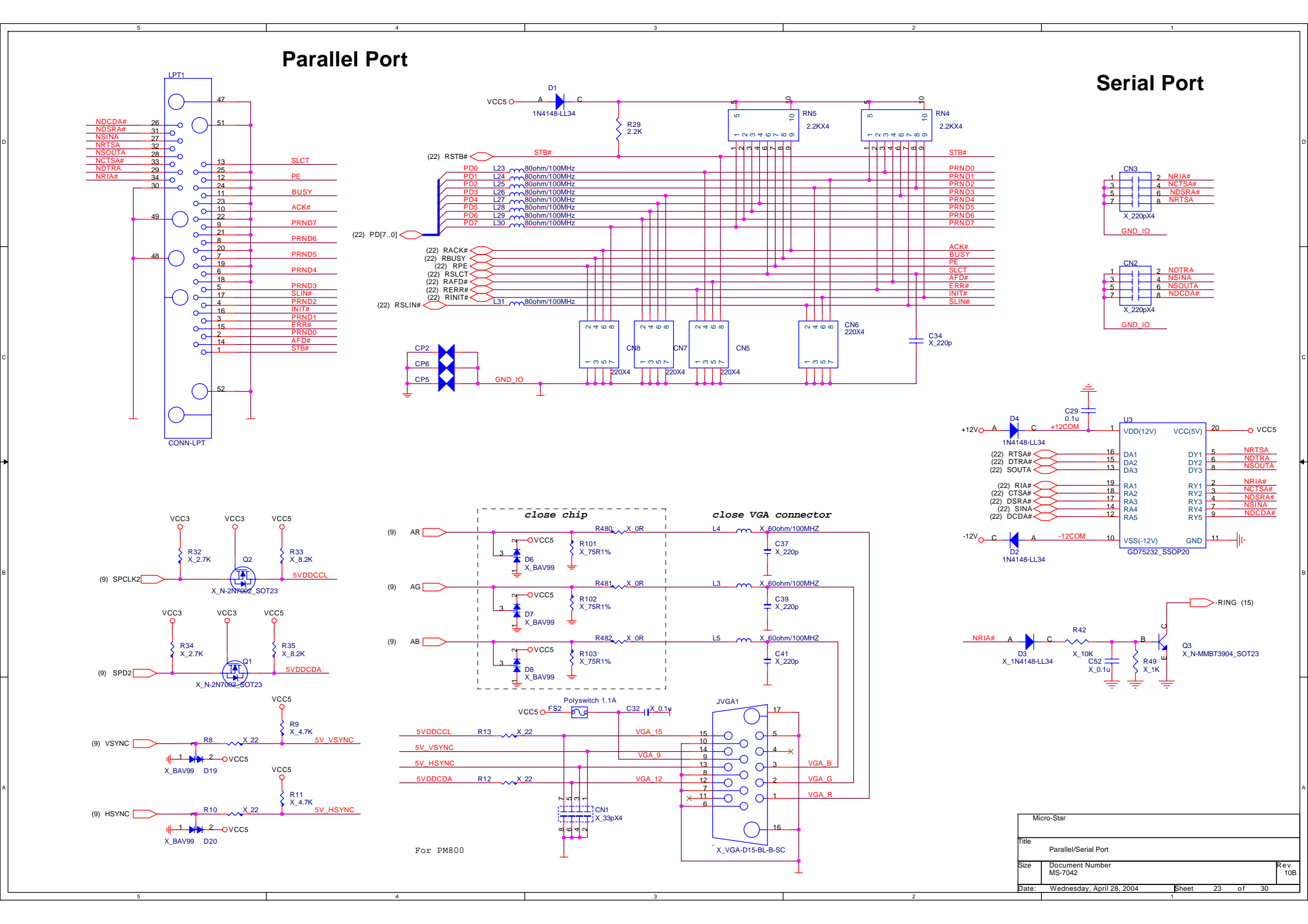
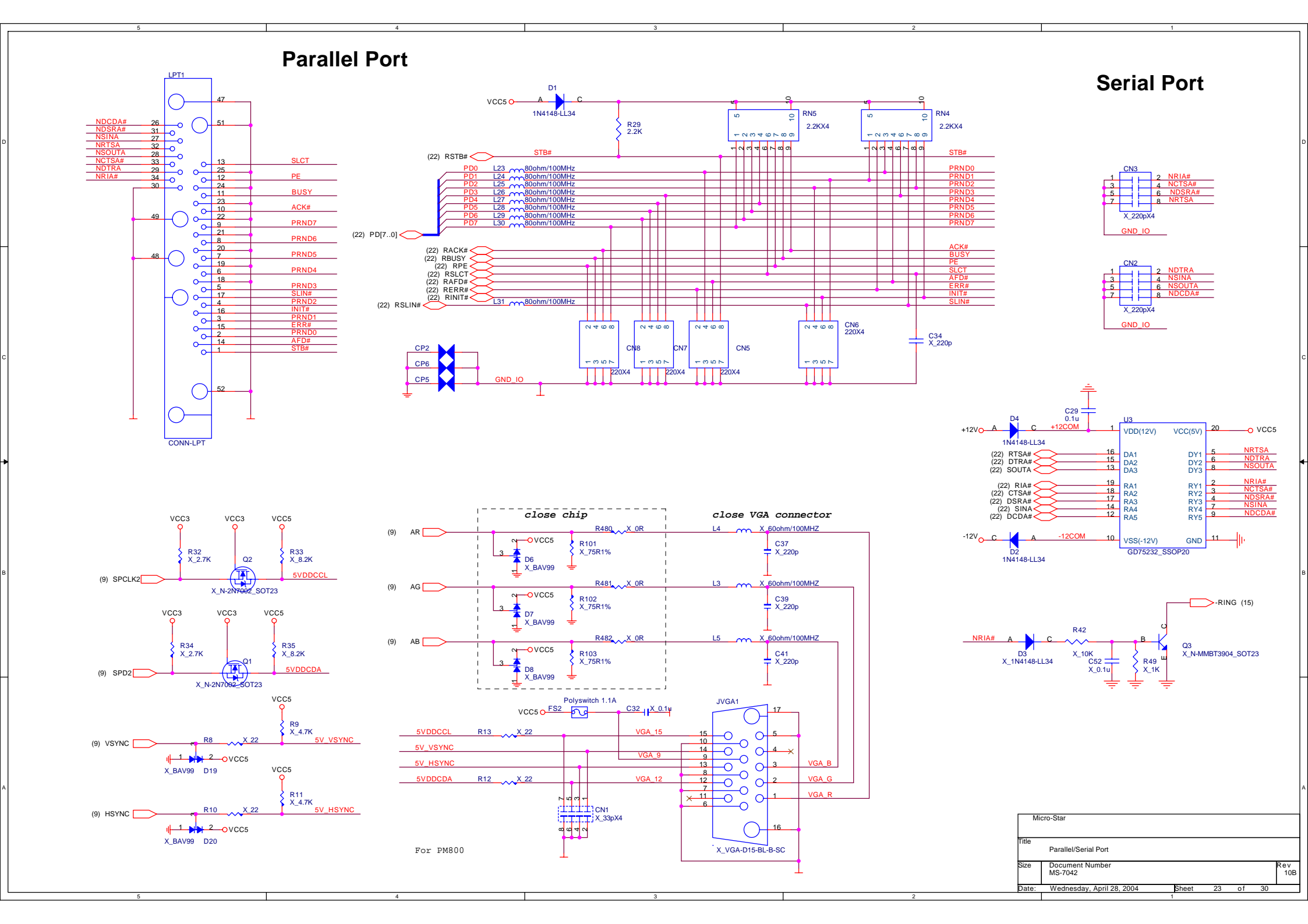
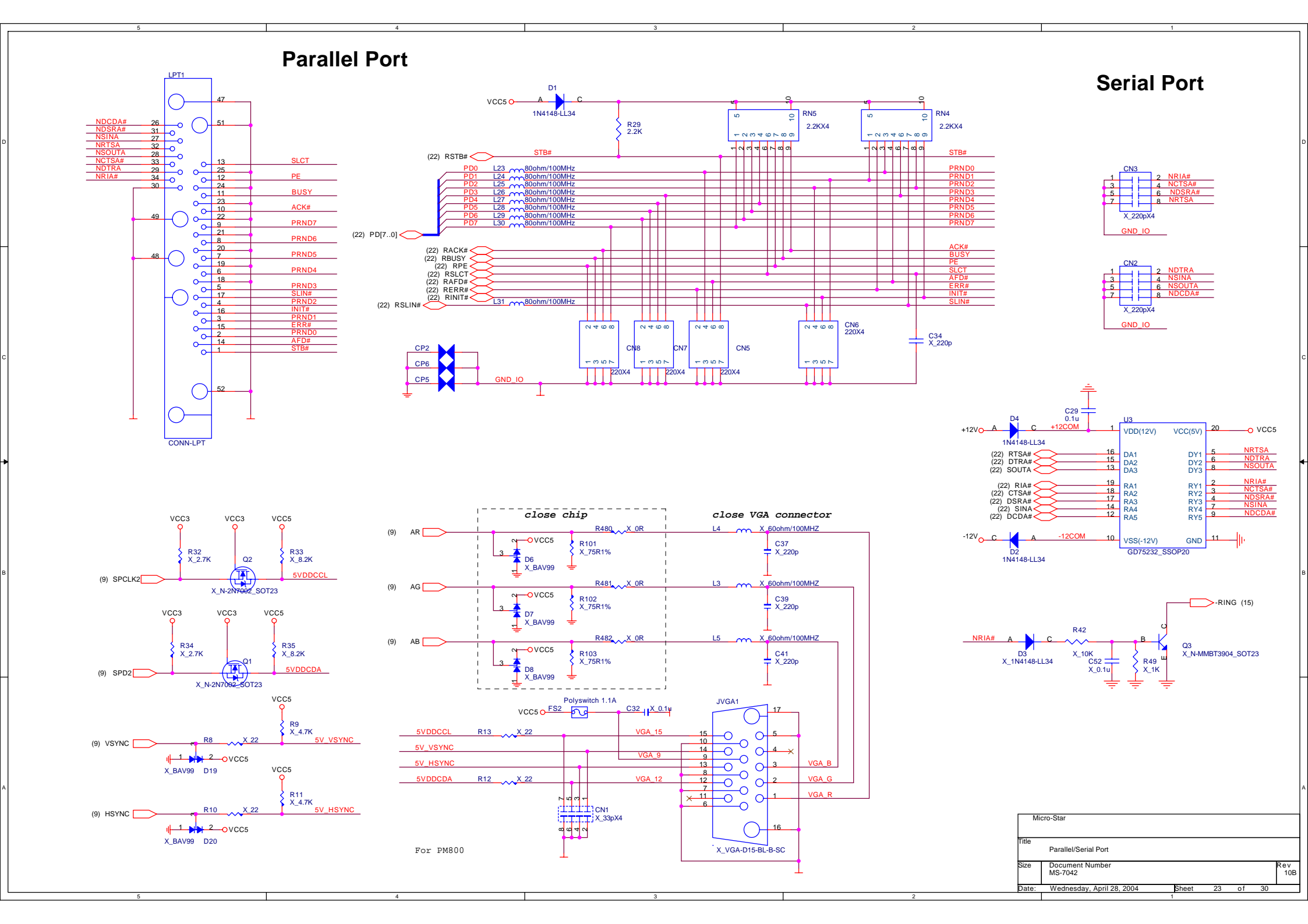
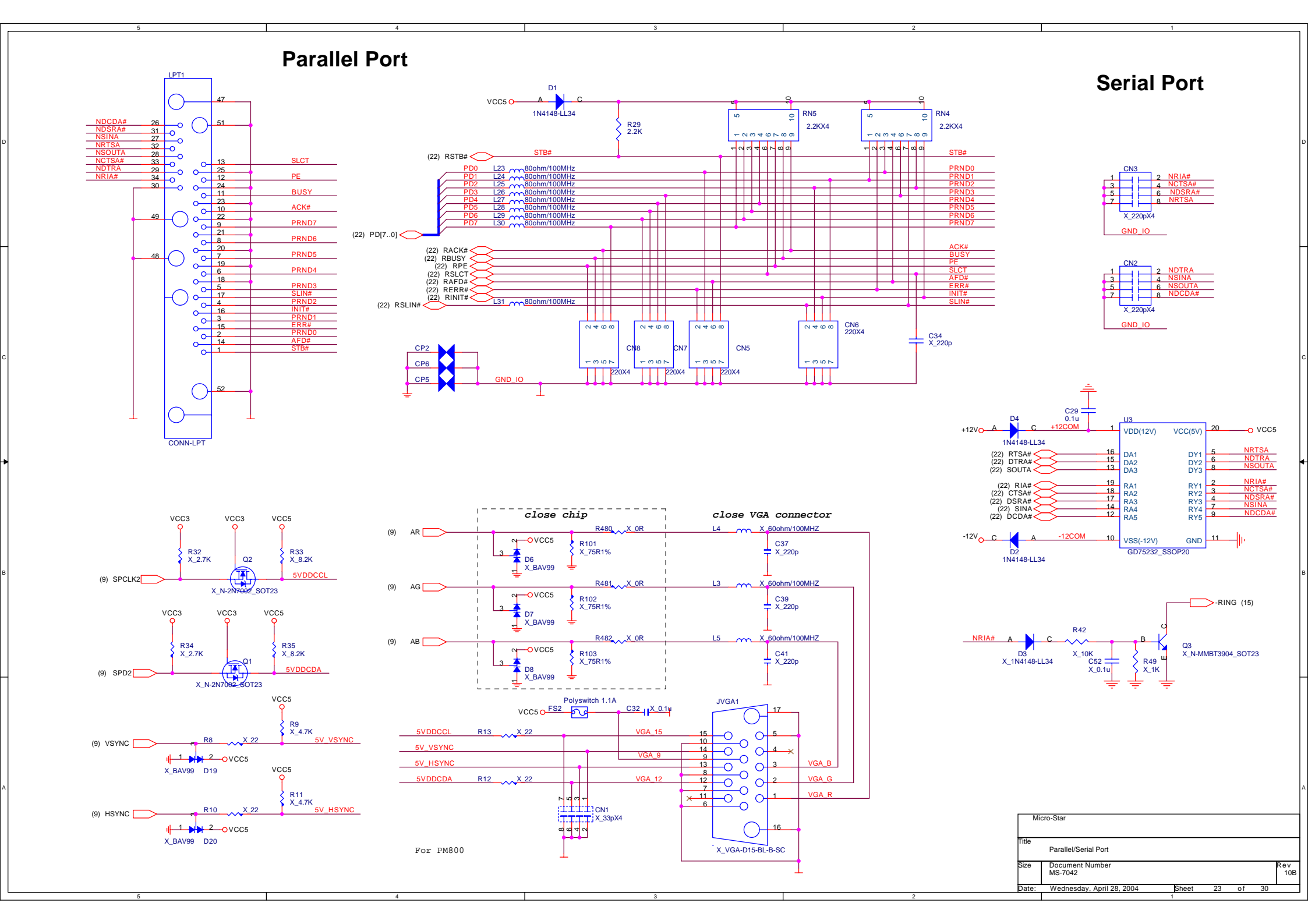
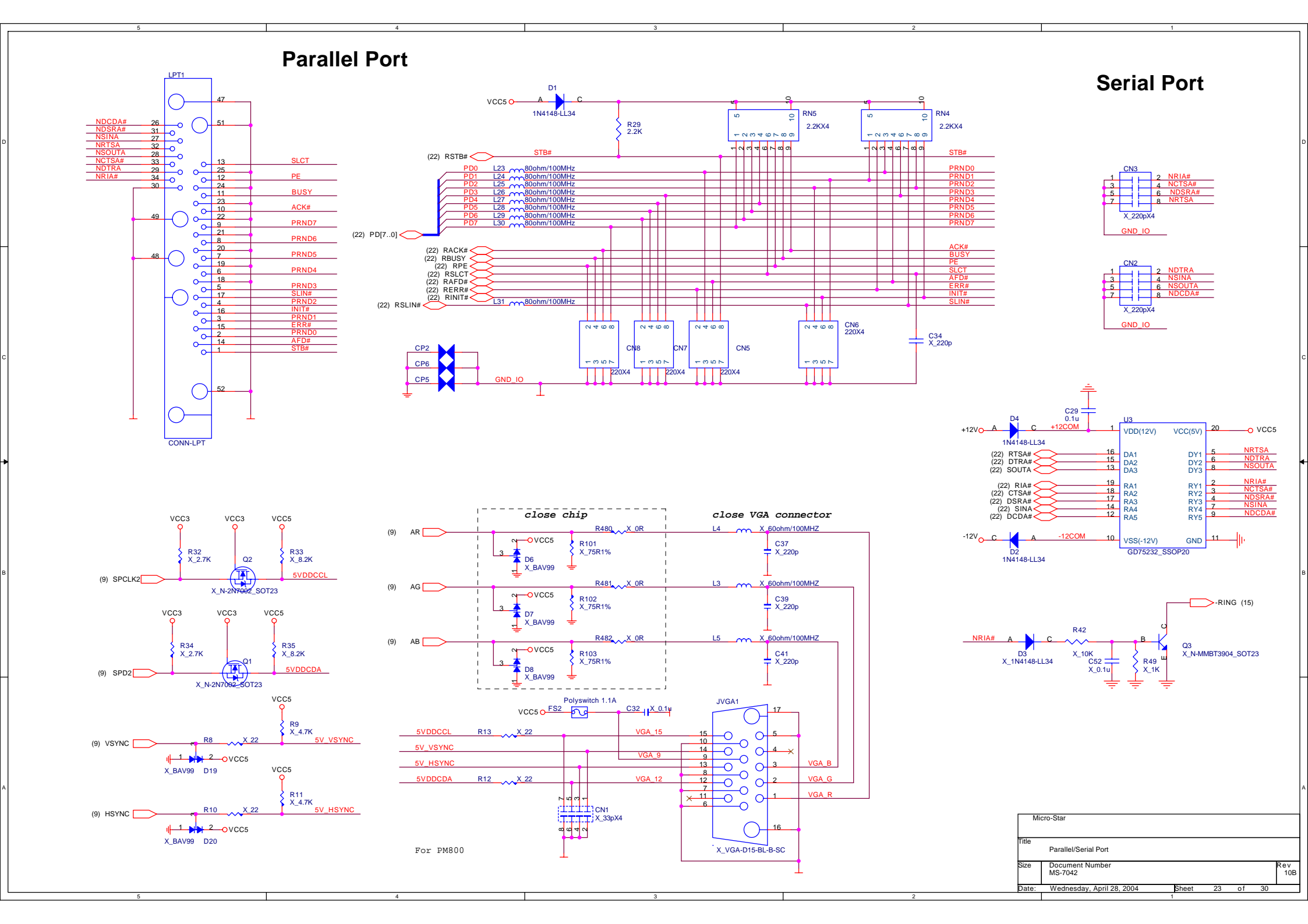
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Parallel Port

Serial Port

close chip

close VGA connector

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Title Parallel/Serial Port

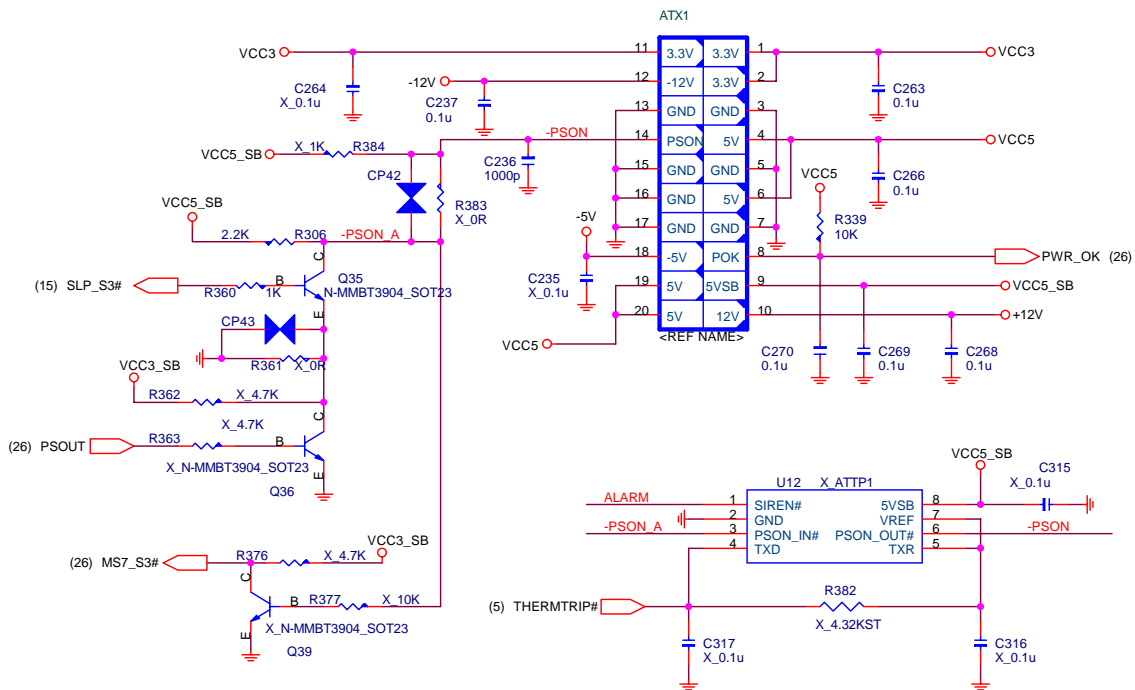
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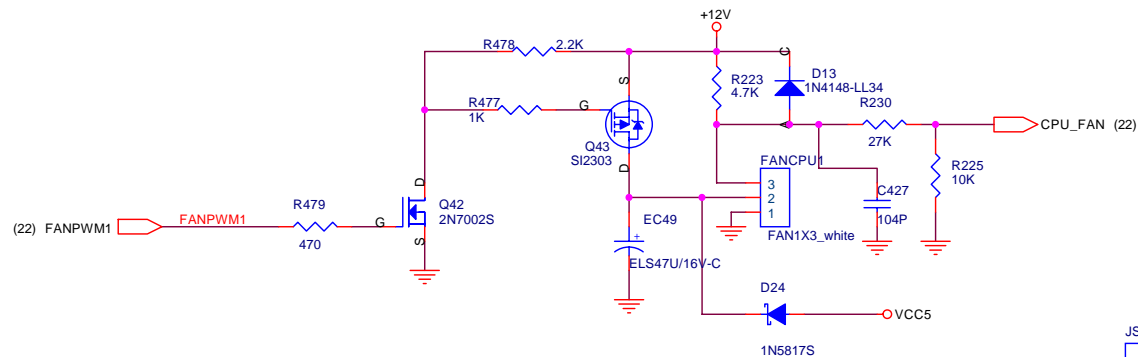
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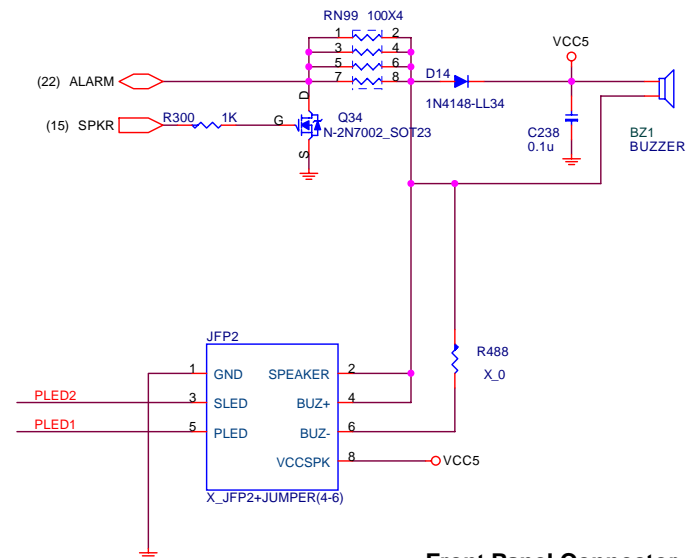
ATX Connector



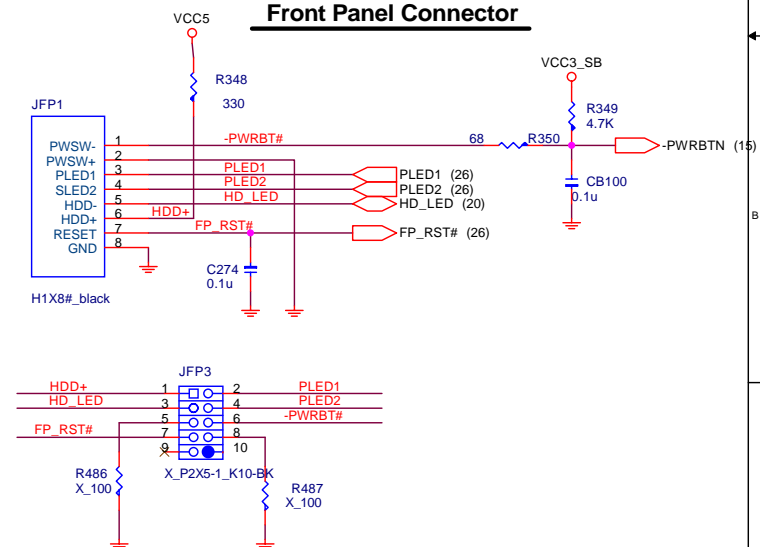
CPU FAN



MSI Front Panel Connector

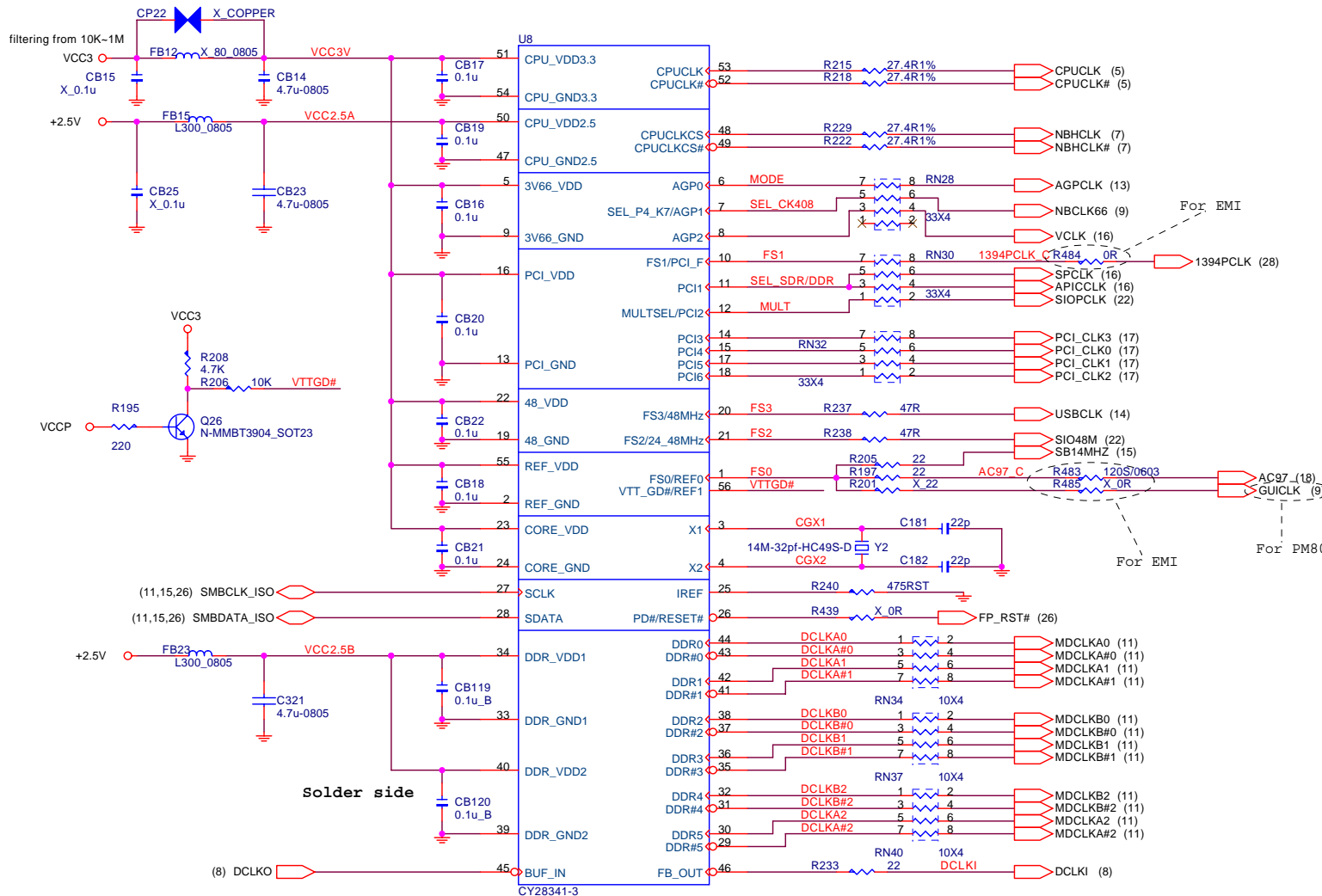


Front Panel Connector

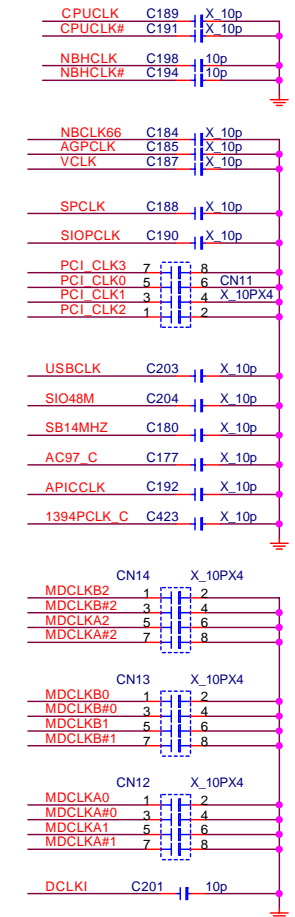


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Title			
ATX Connector & Front Panel			
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Pull-Down Capacitors

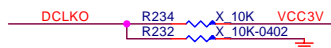


used only for EMI issue
Trace less 0.2"

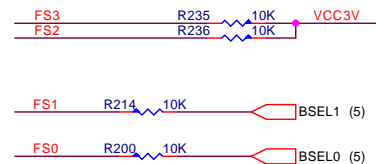
Shut Source Termination Resistors



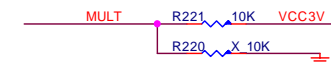
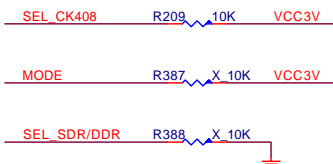
Trace less 0.2" 49.9ohm for 50ohm M/B impedance



CLOCK STRAPPING RESISTORS



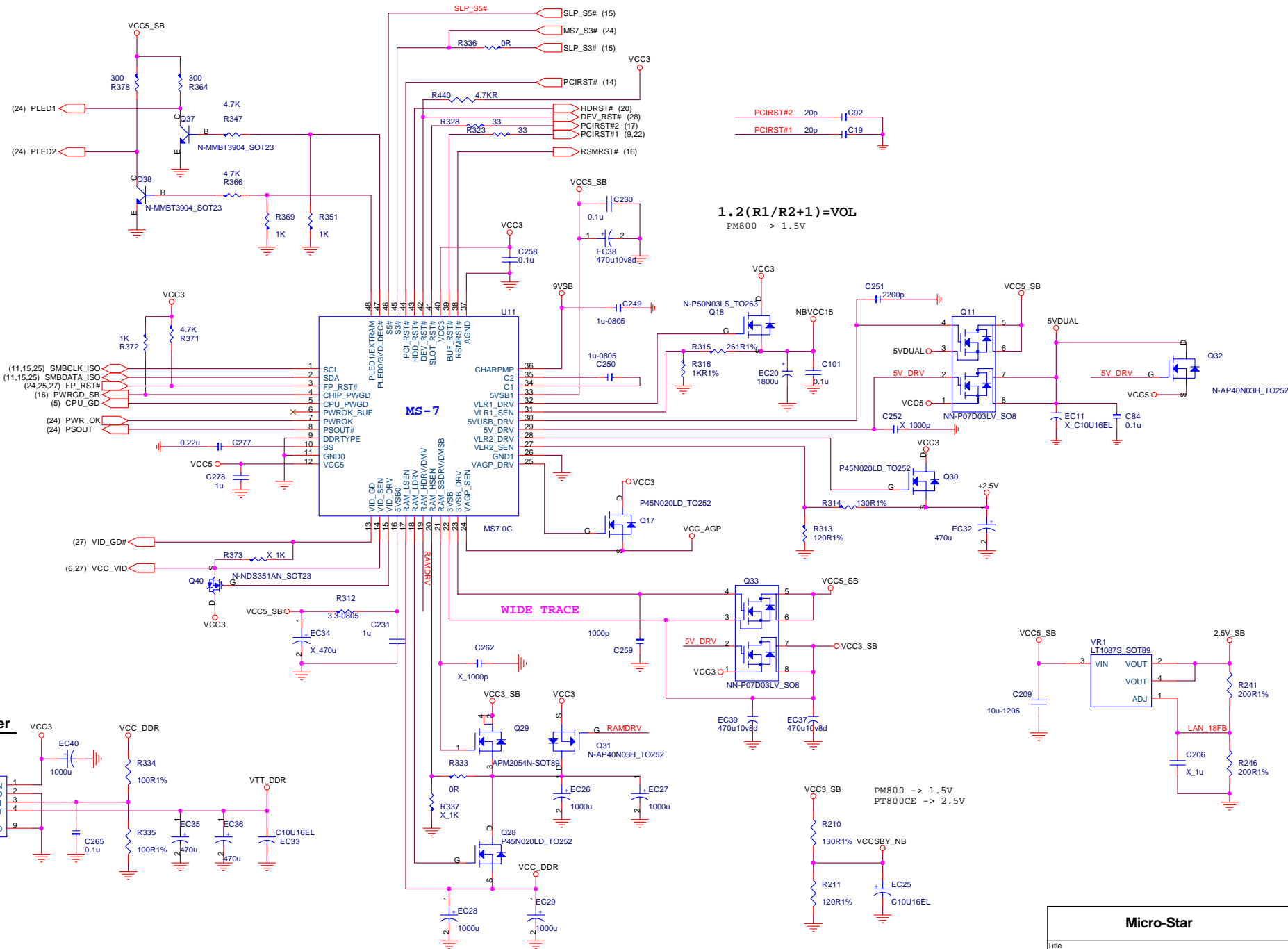
FS3	FS2	FS1	FS0	FSB (MHz)
1	1	0	0	100 MHz
1	1	0	1	133 MHz
1	1	1	0	200 MHz
1	1	1	1	166 MHz



MULT	Rr	Iref	Ioh	Voh
0	221	5.00mA	4*Iref	1.0V
1	475	2.32mA	6*Iref	0.7V

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Title			
Clock Generator			
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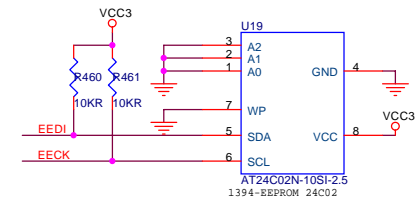
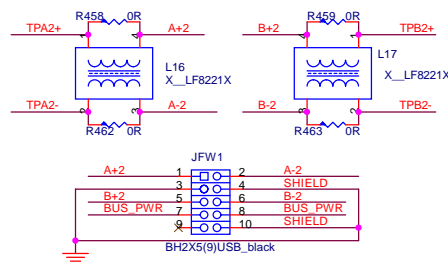
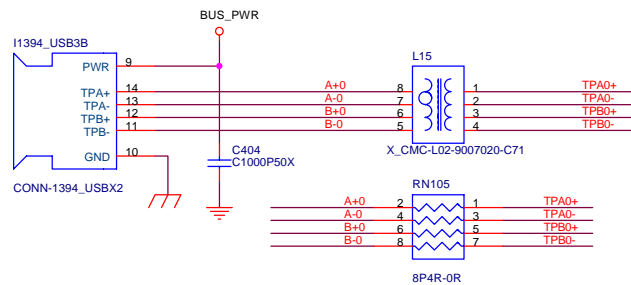
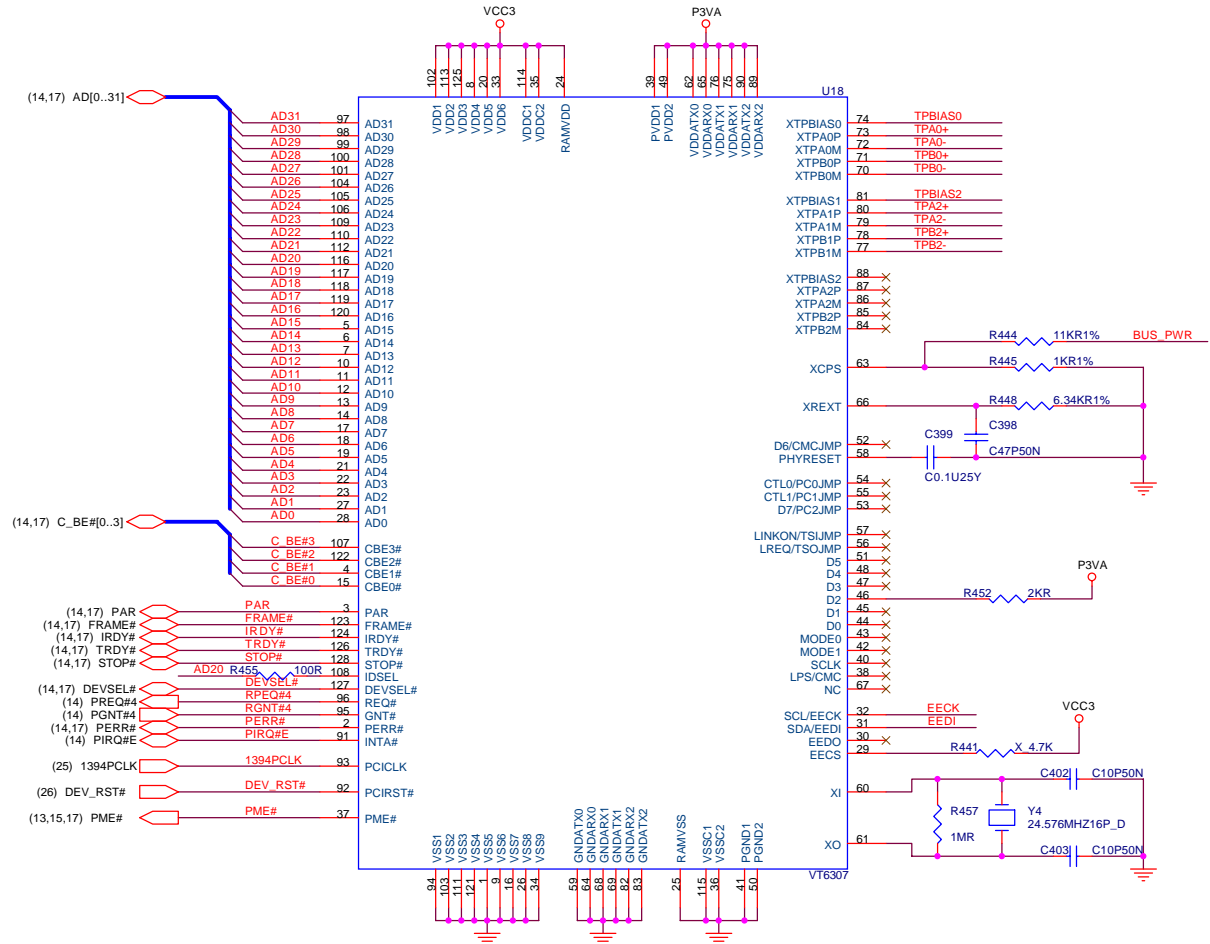
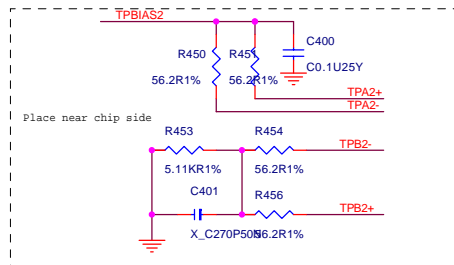
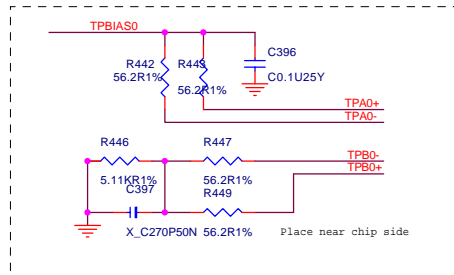
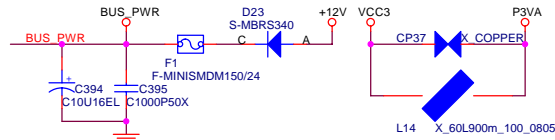
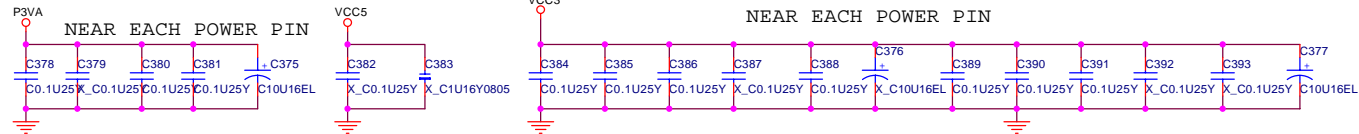
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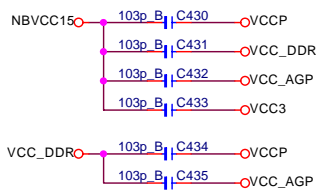
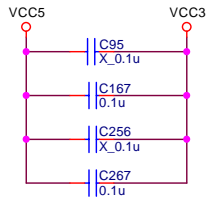
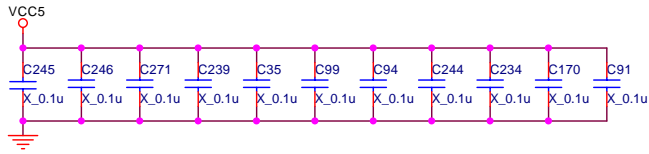
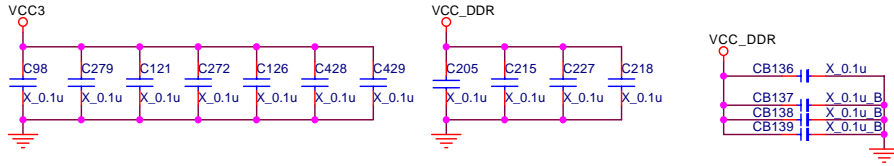


<i>Micro Star Restricted Secret</i>			
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VRM 10 - L6710			10B
Document Number			
MS-7042			
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, April 28, 2004 Sheet 1 of 30	

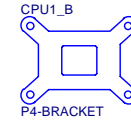
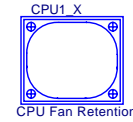
Document Number		MS-7042	
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Wednesday, April 28, 2004	
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IEEE-1394
AD20 PIRQ#E

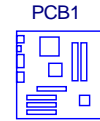
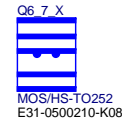
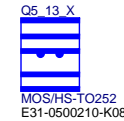
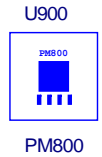




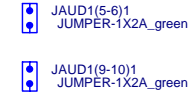
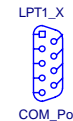
Manual Parts



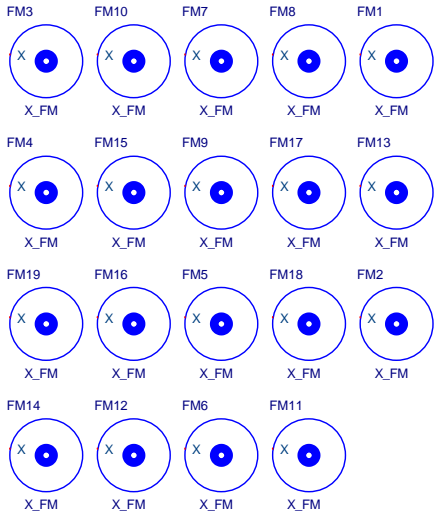
Option Parts



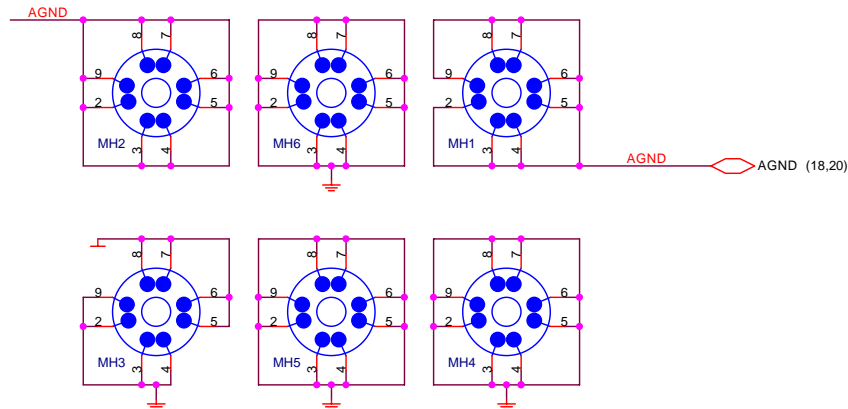
7042 10B



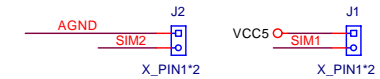
Optics Orientation Holes



Mounting Holes



Simulation



Micro-Star

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EMI PART			
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- Version 0A change to 100 note:
- 1. Remove R441 for VIAL394 EEPROM can flash normally.----Page28
 - 2. Correct JFP1 pin-out direction.
 - 3. Correct VIAL394 front-pin header.
 - 4. Remove R386 for LAN-ID resume normally from S3 state.----Page 16
 - 5. Add L23-L31(80-ohm Bead) for EMI issue.----Page 23

- 10B
- Apr. 12.
- 1. Page 25 : change FB23 to R489.
 - 2. Page 13 : change R140 to 4.7K.
 - 3. Page 14 : stuff CN4 with 180p.
 - 4. Page 11 : CB132, CB134, CB49 --> 33p; CB52, CB135, CB56, CB130 --> 68p by EMI.
 - 5. Page 16 : change R276 to 412 ohm 1% by Via AP note.
 - 6. Page 29 : add C430 -- 435; stuff C167, C267.
 - 7. Page 10 : add C436 -- C439; change CB117, CB105, CB107 to 22u 0805;
 - 8. Page 8 : add C440, C441.
 - 9. Page 14 : add R490.
 - 10. Page 15 : add R491.
 - 11. Page 16 : add R492.

- Apr. 15.
- 1. Page 25 : change R233 to 22; C201 to 10p.

- Apr. 16.
- 1. Page 29 : add CB136 -- CB139 by EMI.

- Apr. 22.
- 1. Page 12 : rearrange DDR termination resistors, R-packs.